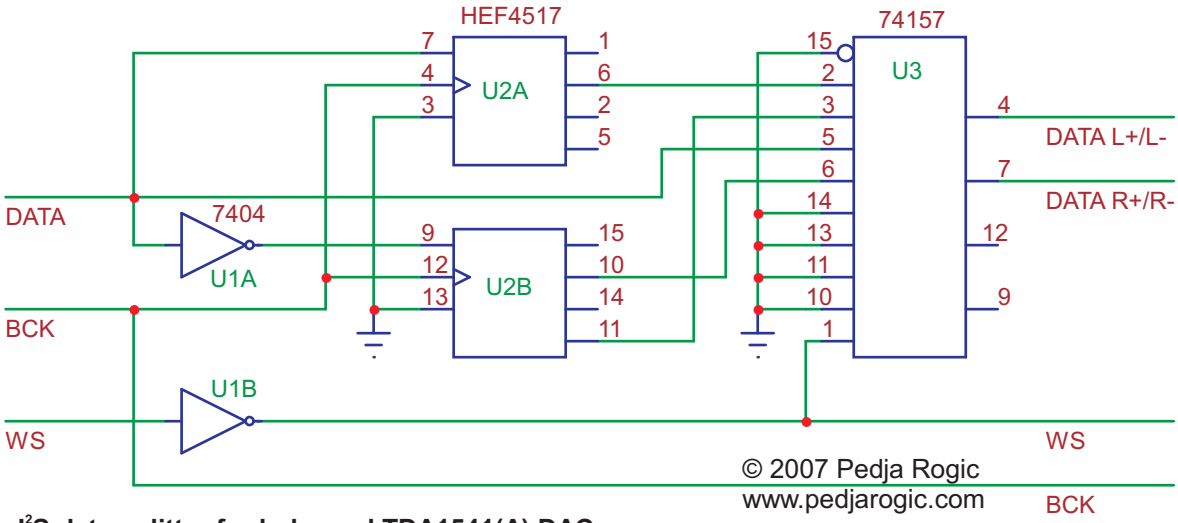
Interfacing balanced TDA1541(A) DAC to CS841x S/PDIF receivers

Fellow interneter has asked me for the interface for the balanced TDA1541(A) DAC fed by the SAA7310. As this chip outputs 32-bit channel subframe, the needed circuit would be actually also applicable with CS8412/8414/8416 S/PDIF receivers. Though the things once or twice got close to that, despite of the shown interest up to now none, to my knowledge, came publicly with such a circuit done with classic logic IC. Instead of dispatching my suggestion by mail I'll post it this way. Those following this site maybe know that I don't like to publish something not tested (and proven to work and sound well) so this would be an exception. For this reason you'll find later explained why the circuit has to work what is supposed to work, but firstly some info on the original references. In fact, I was originally asked about what had to be possibly changed in the previously posted circuit to make it work in the intended environment.

In 1990 HiFi News has published the circuit dividing I^2S data in two separate lines, one for each channel, and each feeding one D/A converter (SAA7321) so each becomes the source of the balanced signal for one channel. Some time ago the circuit has been again brought to the public attention by Ivo (aparatusonitus) and Ray (rfbrw) over at diya. The circuit employs one 74HC132 NOR gate, one HEF4517 64-bit shift register and one 74HC157 two input multiplexer to divide the DATA for left and right channel into the separate lines, filling the space that originally belonged to the other channel's DATA by the inverted DATA of the same channel. Ray points out that the circuit is intended to work only with 16-bit subframes (SAA7220) and suggests use of "4562" (128-bit shift register) if 32-bit subframes are available.

In the other post Ray directs to the figure 28 of the datasheet of AD1852 which points how the original and how target I2S line should look alike. Such a strategy is a bit different and assumes invertion of WS but this way it is possible to accomplish the task with shifts no longer than 64 bits. In other words, with one HEF4517.

So, using this strategy and solving for 32-bit subframe, we have the following circuit.



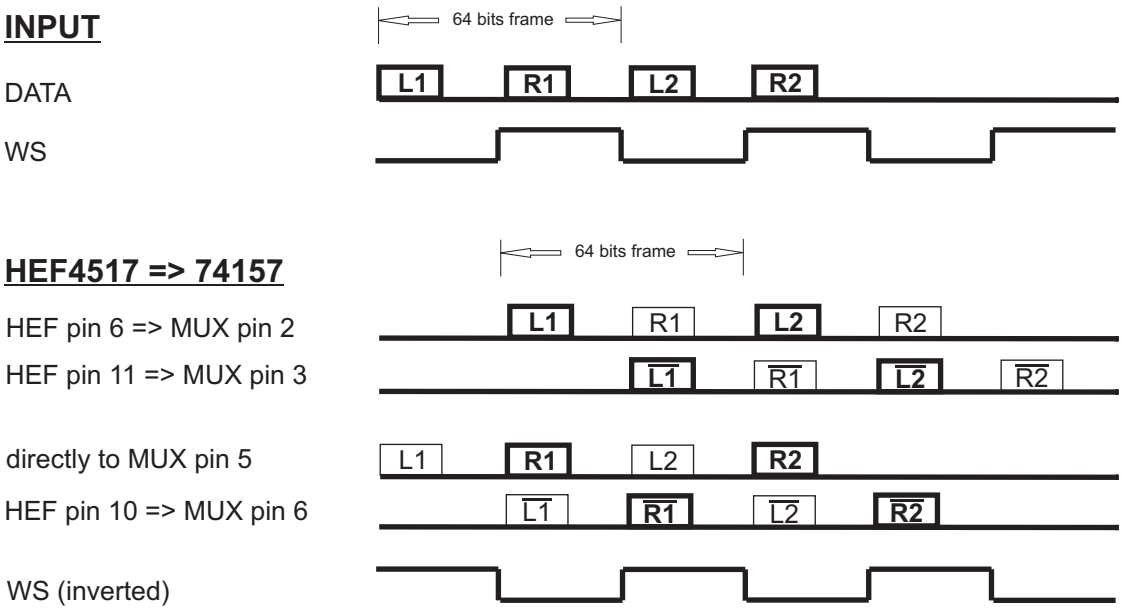
I^2S data splitter for balanced TDA1541(A) DAC

Valid for 32-bit subframe (BCK=64xWS) only!

One may settle on the separate inverters for DATA and WS lines to avoid data related jittering WS by crosstalk but since the output of TDA1541(A) is triggered by BCK this is ultimately not that important.

Shift register delays the left channel data for 32 bits (HEX4517 output pin 6), and the left channel inverted data for 64 bits (pin 11). Right channel data doesn't have to be delayed, and right channel inverted data is delayed for 32 bits (pin 10).

The signals coming out of the pins 6 and 11 of the HEF are then multiplexed; the undelayed signal is multiplexed with the signal coming out of the pin 10 of the HEF. The output of the multiplexer is controlled by the WS: when it goes low the output is updated according to the input I_0 (pins 2, 5) and when it is high the output is updated according to the input I_1 (pins 3, 6). Hence the WS sent to multiplexer is firstly inverted.



As for the output side of the circuit, WS and BCK go to the corresponding pins of both TDA1541(A). Since the output of the TDA1541(A) is updated on the first BCK cycle after the trailing edge of the WS, the WS sent to TDA1541(A)s is also inverted. DATA L+/L- goes to the DATA input of the one and DATA R+/R- goes the DATA input of the other TDA1541(A). The original left channel outputs (AOL, pins 25) of the TDA1541(A)s will give positive poles while the original right channel outputs (AOR, pins 6) will give negative poles of the output balanced audio signal. Of course, you have to take into account possible polarity inversion(s) caused by the active circuits in the DAC output stage.

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