SMD Discrete Diamond Buffer

XEN Audio
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Motivation

You would ask, why yet another discrete diamond buffer ? Aren't there enough of those around ?

You are right. There are tens if not hundreds of discrete diamond buffers [1,2,3,4], all based largely on the LH0002 basic circuit, with various improved current source biasing, etc. In fact, the first mention of the diamond topology dated back to 1964 (application date) in US Patent 3302039 of R.H. Baker. This is very interesting read and to be recommended for those who want a deeper understanding of the thinking behind.

So no, there is no real need for yet another one. Not for normal small signal use, not for driving headphones. In fact, for those applications, the Dennis Feucht JFET Source Follower, and our own DAO power JFET follower, are just as good if not better.

When we were looking for a unity gain buffer for measurement signals of our USB Curve Tracer, we encountered a problem. We have changed the circuit of the Curve Tracer such that it will take a maximum voltage of 60V, and there are basically no high-voltage, unity-gain-stable opamps around other than the OPA445. Nothing wrong also with the OPA445. It is a fine opamp, will take up to 90V, delivers 15mA, reasonably low noise at 15nV/√Hz up to 10Hz at 1kHz, but not quite rail-to-rail, only to within 5V dependent on load. And we thought, we might be able to do better. So we started some information research and simulations.

Circuit & Component Choice

We wanted the buffer to be as widely applicable as possible. The requirements, if we were to do one, would then be :

1) maximum voltage 100V
2) single rail operation
3) rail-to-rail (R2R) to at least within 2V
4) low noise
5) low distortion (<< -90dB for 1Vrms, 10k load)
6) universal (no component change when operating between 20V and 100V).

The rail-to-rail requirement essentially rules out any JFET circuits. They only work properly when there is at least 5V or so head room. And none of the low-noise, high Yfs JFETs will take more than 24V. So it will have to be a BJT circuit, and the diamond buffer is an easy choice, of which the one from Walt Jung [5] is probably the most well-known. There are also many improved versions of the Jung buffer around, mainly using better current sources or sophisticated current mirrors to bias the input transistor pair. But these improvements all eat up voltage head room, and hence go against our R2R requirement. In the end, we cannot think of anything better, and stuck to the Jung basic circuit.

For such simple circuits, the choice of component is key to its performance. We searched around quite a bit before stumbling on the perfect choice for this application – the Toshiba 2SC3324 / 2SA1312 complementary pair. Ultra low noise, Vce 120V, hfe 200 min, SOT23 package, pin compatible with other common BJTs, readily available from Mouser at very affordable prices. What more would you want ? For the LED, we chose a Panasonic SMD 0805 Red (LNJ206R5), but you can equally use others, such as the OSRAM LH R974. Both are available at Digikey, and probably also elsewhere.

We needed to tailor the Jung circuit to suit all the 6 requirements we set out. Because we intended to use multiple output devices in parallel, we thought it would be better to add a base resistor of say 300R for some isolation. The hfe vs. Ic curves of the Toshiba transistors are flat at 2mA, so this is

chosen as the bias point. Effective Re is then about (25/Ic) ~12.5R per transistor. For best thermal tracking, we decided also to use the same transistors at the input and driver stages with the same bias and emitter resistor. Going to a higher value for the emitter resistor will reduce distortion somewhat, but at the expense of higher Zout. So we decided to stick to 10R, but use two pairs of transistors in parallel for the driver stage. This will give a Zout of about 5.5R, and the buffer will remain in Class A with I out up to 4mA.

To satisfy requirement 6, we replaced the LED biasing resistor with a current regulating diode. Here we chose the Semitech S-202T for its small package. It is a bit expensive, but available at Mouser. You can always replace it with a 1206 resistor which is of similar physical size. But you need to adjust its value for various rail voltages. Our PCB is compatible for both.

To set the input stage bias to 2mA, we need to change the value of the current source degeneration resistors from 220R to 470R. Also in order to save space, we removed all the protection circuits of the original Jung schematics in pour first prototype. So in case of a short circuit, the output transistors are likely to blow. Later on, we did however managed to put back the 4 protection diodes in, without increasing PCB footprint. (Schematics V1a, Appendix 1)

Otherwise, the circuit is identical to that published by Jung. We decided also to leave out the input and output resistors, so that the user has the freedom to match its value to the application. For power rail coupling, we placed a WIMA SMD 2824 polyester cap of 220n 100V closed to the output transistors. Bulk eletrolytics should additionally be placed on the main PCB close to the buffer module.

People who know us from FET based circuits know that we are fanatic with matching. Here it is no exception. We matched the LEDs, all transistors for Vbe at 2mA Ic, as well as hfe at the same bias current. For the small batch of those we obtained from Mouser, the voltage variations of the LEDs were excellent (within 4mV). The hfe varies quite a bit for the BJTs, especially for the PNP. Also the PNPs have on average higher hfe (around 320) than the NPNs (around 280). But I think the circuit will still function very well even without any matching of the BJTs at all.

Simulations

Since Spice models are readily available for all active devices, we started off by a quick simulation first before building. Using +/-30V rails, we can get close to 28.5V without any noticeable clipping. At 1Vrms 1k load, THD is -114dB (about equal 2nd & 3rd). But even at 40Vp-p and 5k load, THD is still an excellent -94dB. This is impressive by any standard, especially at large amplitudes. Note that 40Vp-p and 5k load corresponds to the limit of Class A operation. Even when it is totally out of Class A with a 2k load, THD is still an impressive -88dB.

Frequency response is also excellent in simulation, with -3dB bandwidth over 100MHz.

PCB Layout

To ensure lowest DC offset, it is essential that all transistors track each other thermally, especially within each half of the circuit. The symmetrical nature of the circuit also lends itself to using the same layout on each side of the PCB, one for the top half and one for the bottom half. A 4-pin DIL header provides output interface to the outside world, with the 4 pins being +Vs, Vout, Vin, and -Vs. This way, you can either use a single row DIL header, or hard wire them onto a DIP-8 socket to make it pin compatible with standard opamps.

A small heat sink was also manufactured for the module using CNC wire cut EDM. This has a footprint of 12x10mm, with a height of 20mm. The large height is largely due to the SMD cap. Otherwise we would have got away with 14mm only. The heat sink is divided into two identical halves. This allows very easy potting of the entire circuit using thermal conductive potting components (ceramic based, electrically non-conductive). The components are so chosen that the transistors protrudes the most from the PCB and hence has the closest contact with the heat sink inner surface.

Measured Performances

The prototype worked first time. With supply rails of +/-12V and no trimming at all, offset voltage was 6mV. It drifts a maximum of +/-2mV over a period of over 30 minutes. And this is without the special heat sink used to thermally couple all devices and increase thermal inertia. We did not consider trimming necessarily, though this can surely be done.

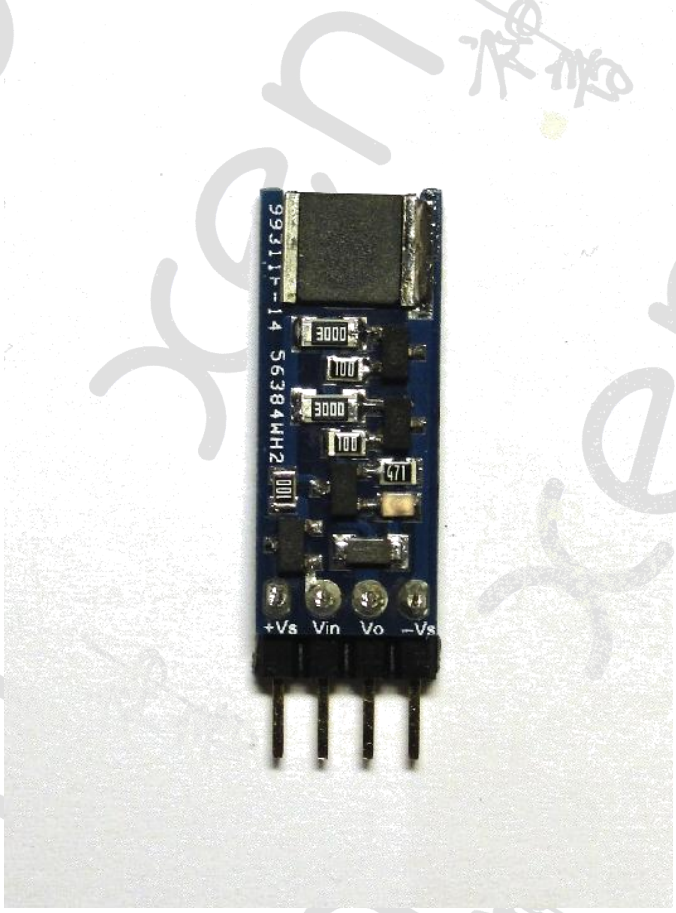
We have no problems getting outputs to within 1.5V of both rails. Our functions generator is not high voltage enough to test higher signal than 12V, but we expect same result for higher rail voltages.
Square wave response to 10kHz is perfect, with no overshoot at all. Frequency response is flat to 2MHz which is also current limit of our test equipment. For audio use this is more than sufficient, but we shall try to find equipment to do further test on this. Small signal (2.5Vrms) distortion is well below 90dB, again limited by our test equipment. As above, we shall try to make better measurements and report back. Driving a 10k load, gain is 0.99.

So all in all, it delivers all it promises, and we consider this a very nice device with a lot of useful applications, and at very moderate costs.

Possible Variants

In a private communication with Walt Jung, he suggested that the input device be bootstrapped from the emitters of the output devices (see Schematics Version 2, Appendix 1). This can also be implemented in the current layout without too drastic changes. However, as we are using the same devices throughout, where they see the same voltage and bias current, they track each other perfectly against any thermal drift in the current version. This is no longer the case in the bootstrapped version, as the input devices (Q1, Q2) will see much less voltage, and the bootstrap devices (Q3a, Q4a) will get double the current. So we decided to stick to Version 1.

All tributes to Walt for sharing with us such a simple yet outstanding circuit.

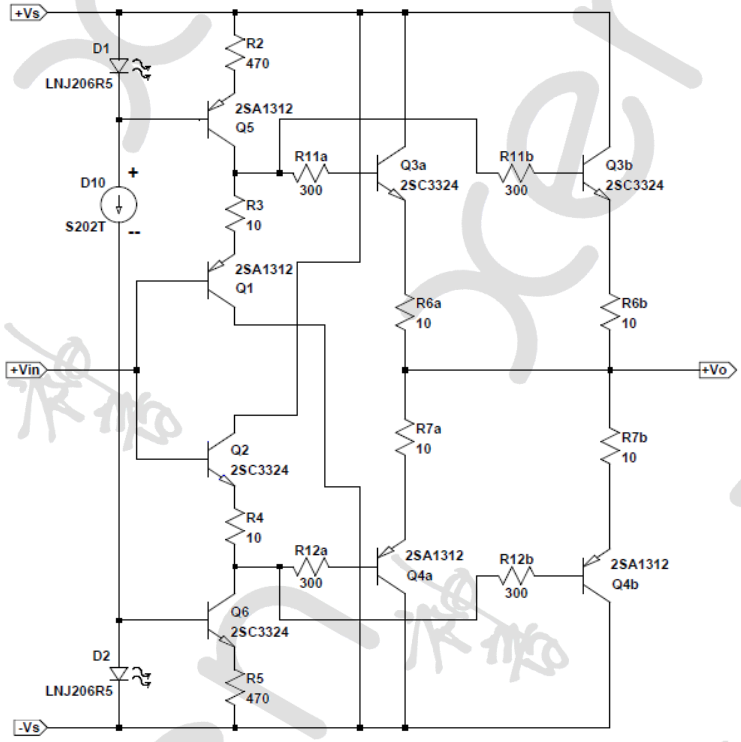


References

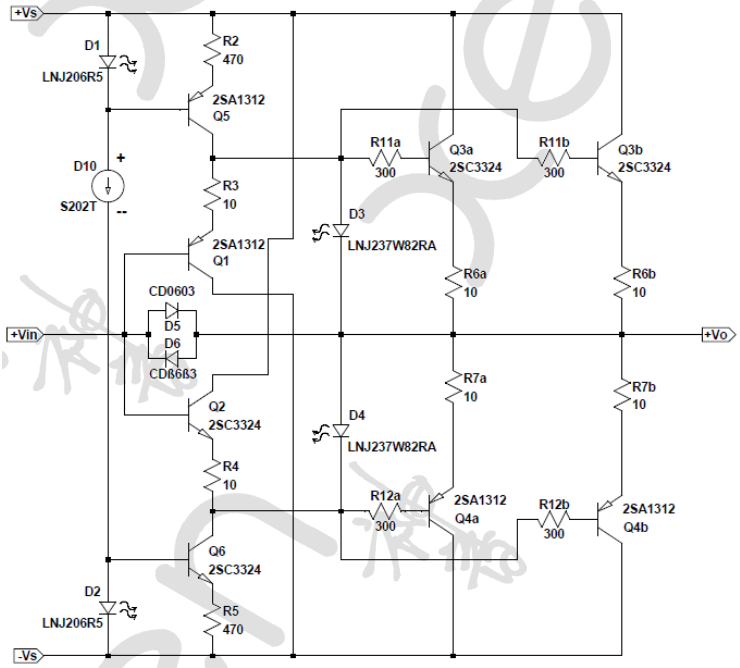
1. http://www.diamondstar.de/dDB_overview.html
2. http://www.diyaudio.com/forums/parts/97959-diamond-buffers.html
3. http://www.cavalliaudio.com/diy/cth/main.php?page=design/opdesign
4. http://cdn.head-fi.org/8/8f/8f6b5846_mainke2.gif
5. http://waltjung.org/PDFs/WTnT_Op_Amp_Audio_2.pdf

Appendix 1 Schematics

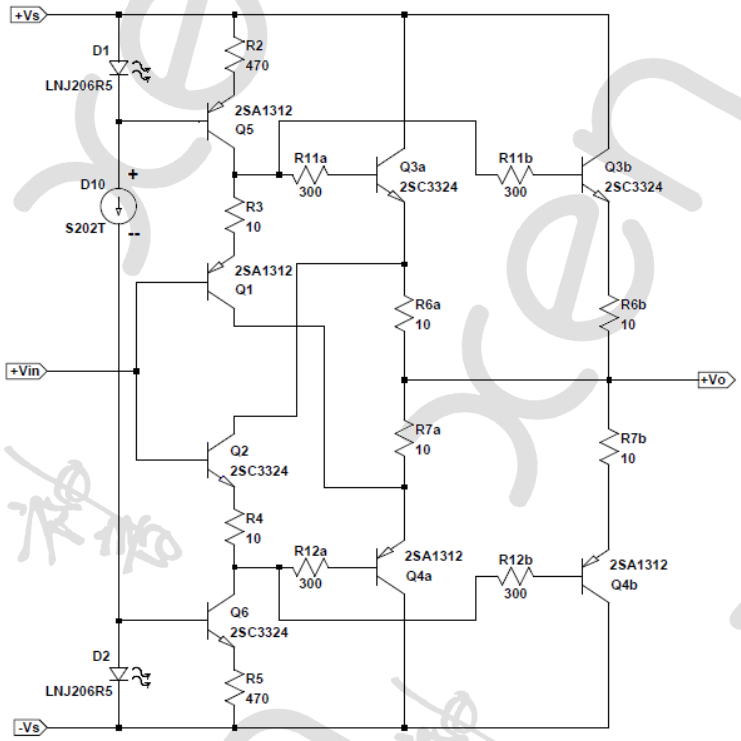
Version 1 as built



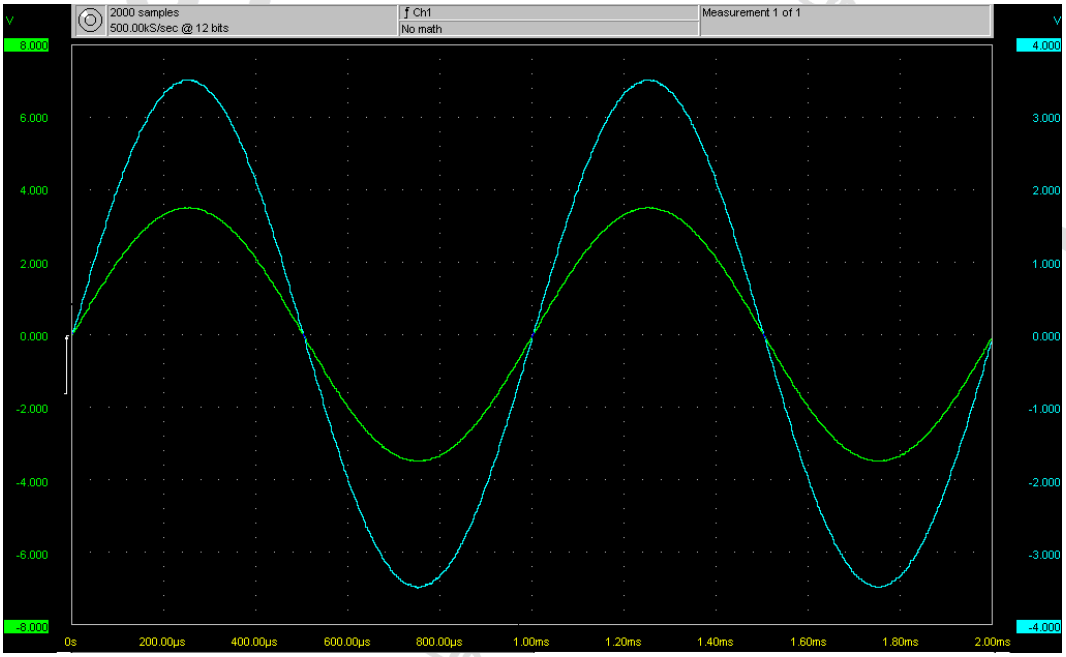
Version 1a with Protection Diodes



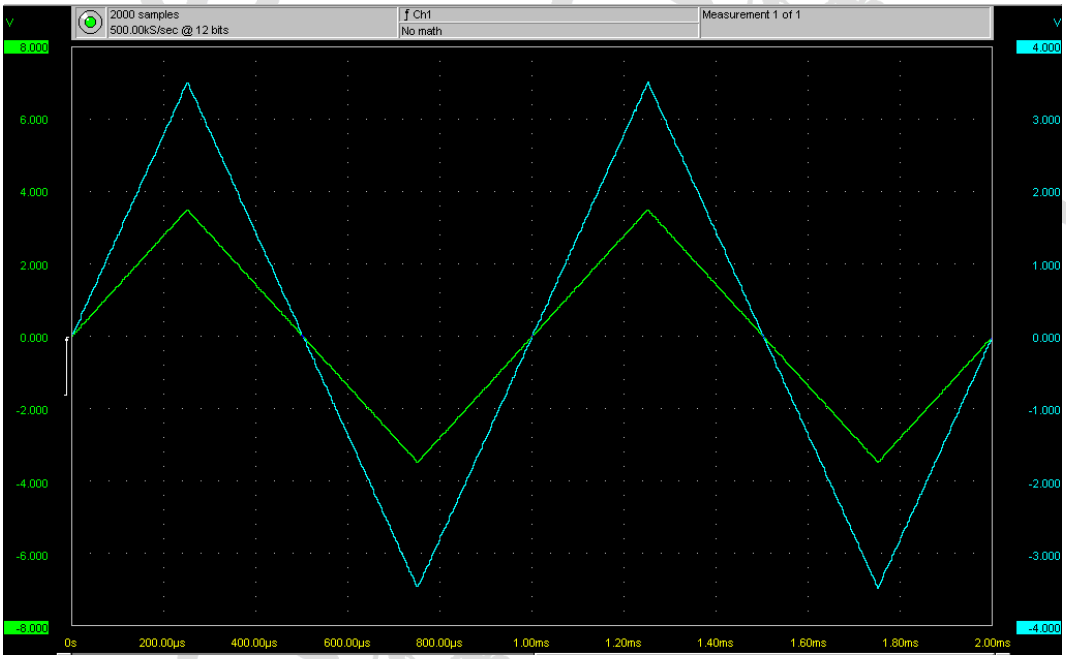
Version 2 proposed Output Bootstrap



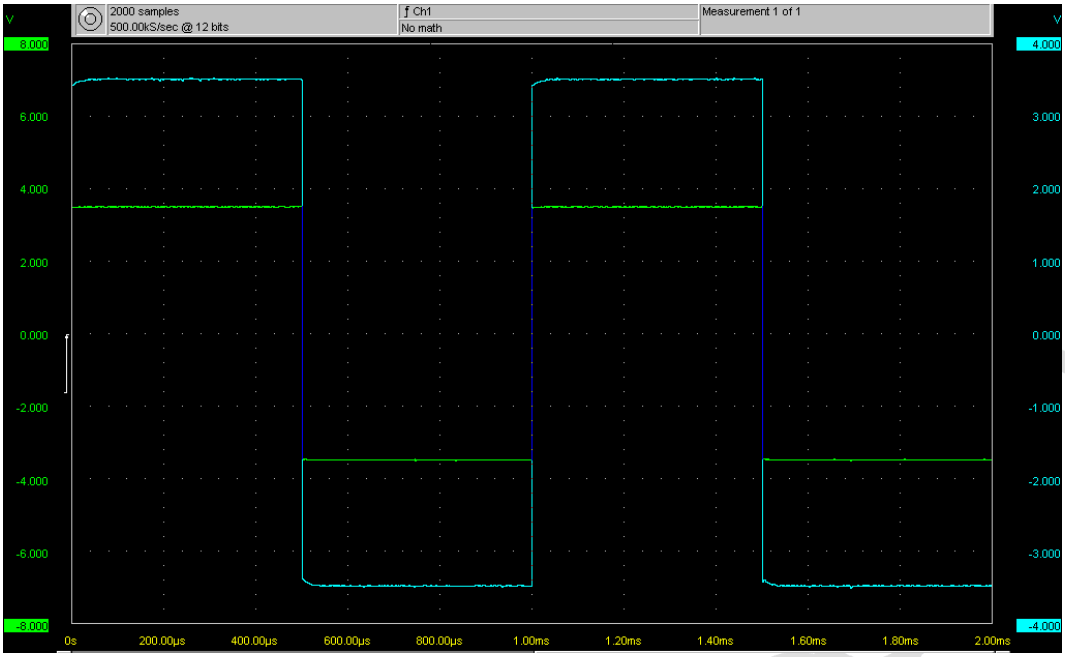
Appendix 2 Measured Performances



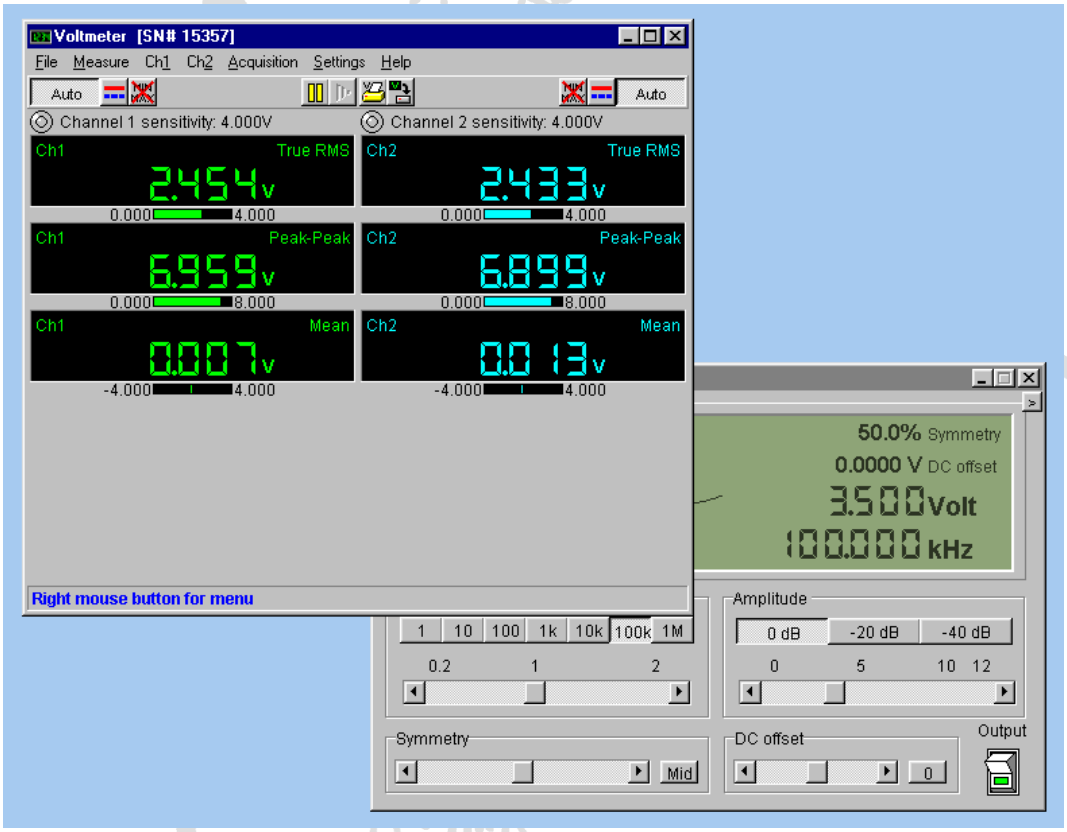
10kHz Sine Wave
(Green = input, Cyan = output)



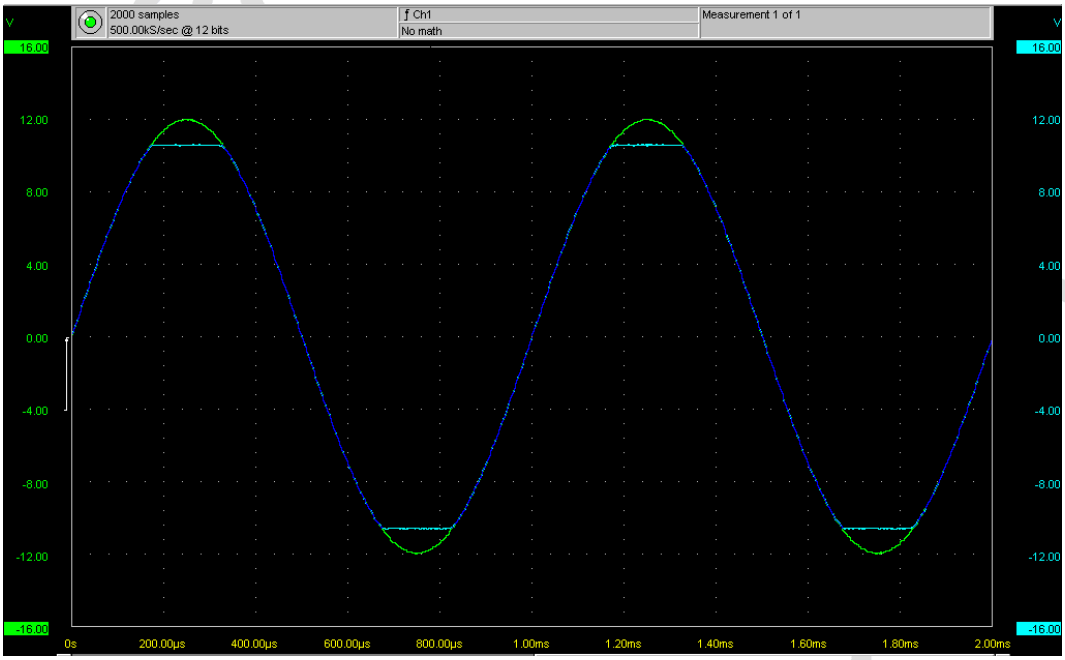
10kHz Triangular Wave
(Green = input, Cyan = output)



10kHz Square Wave
(Green = input, Cyan = output)



DC & RMS Voltages
(Ch1 = input, Ch2 = output)



Clipping
(Rail = +/-12V, Green = input, Cyan = output)