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1 Introduction

Two-way radio applications typically use sub-audio tones to control the squelch path. These sub-audio tones are commonly referred to as CTCSS (continuous tone controlled squelch system) tones.

A common problem in two-way radio applications occurs during receipt of the CTCSS tone. The detection time for a CTCSS tone is typically on the order of 250ms. Since the receiver's speaker path is closed until the CTCSS tone has been detected, up to 250ms of incoming speech can be lost during this time.

CTCSS detection time cannot be reduced to zero, and this means that the possibility of dropped speech prior to CTCSS detection cannot be eliminated.

One technique to minimize this situation is to delay the transmission of voice until the receiver's expected CTCSS detection time has elapsed. This will ensure that no voice is present at the receiver until the CTCSS tone has been detected and its speaker path has been opened.

This application note presents one possible method for performing this technique. The CMX639 CVSD voice codec is used to encode the voice into a serial data stream, which is then passed to a memory IC for storage. After a user-selectable time delay has elapsed, the encoded voice is passed back to the CMX639 for decoding, and the recovered speech is then passed to an external speaker circuit.

The CMX639 datasheet, which can be downloaded from www.cmlmicro.com, should be consulted while reviewing this application note.

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2 Overview

The schematic diagram shown in Figure 1 is an audio delay circuit based on the CMX639 CVSD voice codec. In addition to the CMX639, the circuit uses a Cypress CY7C187 64K x 1 bit SRAM IC, two binary counters and a hex inverter chip to provide a maximum delay of 1.024 seconds. This circuit is designed to provide a starting point for a designer who wishes to implement an audio delay circuit in their application. Since audio input sources and output destinations are application dependent, details about those functional areas have been omitted from the circuit.

Figure 1 includes pinouts for plastic dual-in line (DIP) packages to facilitate prototyping. Surface-mount packaging can be easily substituted if production quantities are required.

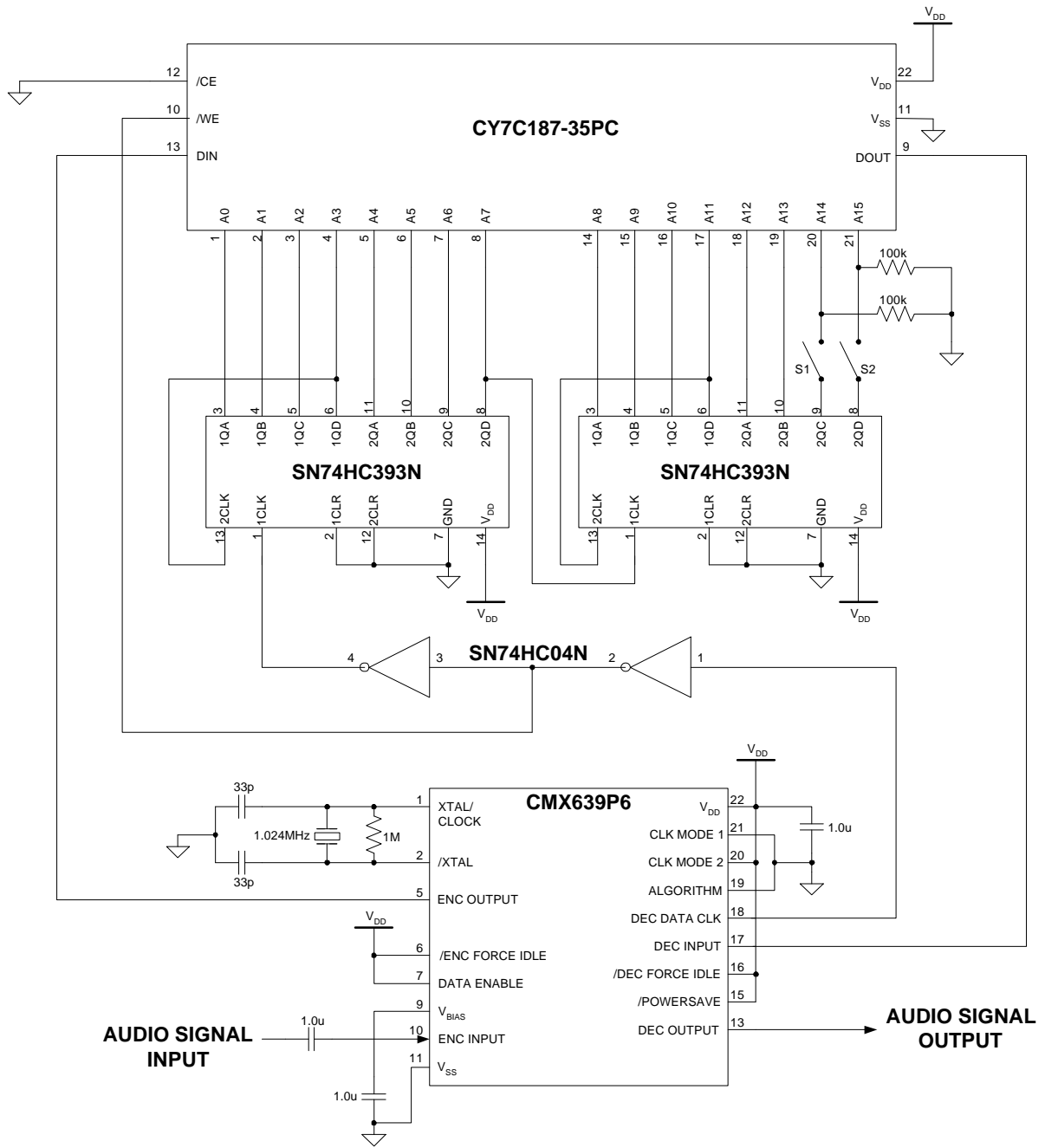


Figure 1, CMX639 Audio Delay Circuit Diagram

3 Description of Circuit Operation

3.1 General Comments

3.1.1 CMX639

The CLK MODE 1 and CLK MODE 2 pins set the sampling rate of the CMX639 to 64kbps. The /ENC FORCE IDLE, /POWERSAVE, and /DEC FORCE IDLE inputs are tied to V_{DD} to set them inactive. The DATA ENABLE input is tied to V_{DD} to make the encoded data available at the ENC OUTPUT pin. The ALGORITHM input is tied to V_{SS} to select a four-bit companding algorithm for optimal sound quality.

The CMX639 requires a “master” timing source at its XTAL/CLOCK input during operation, and this timing source can vary between 500kHz – 2.048MHz. The CMX639 internally generated sampling rates, filter bandwidths and associated parameters are based on the use of a 1.024MHz timing source. The use of any other frequency at the XTAL/CLOCK input will result in a proportional scaling of these parameters.

For example, Figure 1 has the CMX639 configured for a 1.024MHz XTAL/CLOCK input and a 64kbps internally generated sampling rate. If the XTAL/CLOCK input is reduced to 1.0MHz, the actual internally generated sampling rate will be 62.5kbps. Another noteworthy item for this example is that the encoder/decoder passband will shift down in frequency from 300-3400Hz (1.024MHz XTAL/CLOCK input) to 293-3320Hz (1.0MHz XTAL/CLOCK input).

Customer feedback indicates that 1.024MHz crystals are difficult to obtain without custom crystal orders and large purchase commitments. There are several options that can be explored to overcome this situation.

A relatively inexpensive option involves the division of a higher frequency to a lower frequency that is useable by the CMX639. For example, an inexpensive 4.096MHz crystal can be divided by four to produce a 1.024MHz clock signal. Another option involves other crystal frequencies, such as 1.0MHz and 2.0MHz, which may be more readily available (and therefore less expensive) than 1.024MHz crystals. This approach must be used with caution, however, as clock signals other than 1.024MHz will cause scaling of many CMX639 parameters. Yet another option involves the use of clock oscillator ICs as the timing source for the CMX639. One concern with this approach is the drive level of the oscillator. The CMX639 requires a XTAL/CLOCK input signal with amplitude of at least 40% V_{DD} peak to peak. Simple logic devices such as inverters can be used to boost the amplitude of these timing signals if necessary.

The output impedance of the source that drives the CMX639 ENC INPUT should be less than 1k Ω to minimize noise in the recovered audio.

The other CMX639 inputs are the same as those illustrated in the “External Components” section of the CMX639 data sheet.

3.1.2 SRAM Memory IC

The Cypress CY7C187-35 64k x 1-bit SRAM chip was used in this circuit to store the one-bit-per-sample serial data stream from the CMX639. Since the bit time for the 64kbps audio data stream was much greater than the maximum access time of the SRAM IC, the slowest version of the CY7C187 ("-35") was adequate for this design. This SRAM IC is also available from IDT and Performance Semiconductor.

The /WE (write enable) signal is controlled by a delayed version of the CMX639's decoder data clock signal. The address of each data write is determined by the address formed by the two SN74HC393 counter ICs. Writes are made to the SRAM when the /WE is low, and reads are made from the SRAM when the /WE is high.

The data bit corresponding to the address from the previous cycle is made available at the DOUT pin when the /WE is high. For example, when address 1 is assigned by the counter IC and /WE is high, the bit previously stored in address 1 is made available at the DOUT pin. When the /WE then transitions low, address 1 is still selected, and the data at the DIN pin is written into the memory at address 1.

The net effect of this situation is that a bit written into memory will be read out in $(2^N - 1)$ decoder data clock cycles, where N = the number of bits activated in the cascaded binary counter ICs.

The /CE (chip enable) input is tied to V_{SS} so that the SRAM IC is permanently selected.

3.1.3 Binary Counters

Two Texas Instruments' SN74HC393 dual 4-bit binary counter ICs are used to create addresses for SRAM reads and writes. Each SN74HC393 is configured so that its dual 4-bit counters are combined into a single 8-bit counter. The two SN74HC393s are cascaded to create a 16-bit counter that yields a maximum of 2^{16} addresses ($2^{16} = 65,536$ addresses).

Switches S1 and S2 are applied to the two most significant bits of the second SN74HC393 IC. These switches allow varying amounts of time delay to be introduced in accordance with the following table:

Switch S1	Switch S2	Resulting Delay (seconds)
Open	Open	0.256
Closed	Open	0.512
Closed	Closed	1.024
Open	Closed	Not allowed

Table 1, Adjustment of Audio Time Delay

3.2 Overall Operation

The audio signal to be delayed is applied to the ENC INPUT pin of the CMX639. The CMX639 converts the audio signal into a 64kbps serial data stream using CVSD voice coding. The resulting serial data stream is then passed from the CMX639 ENC OUTPUT pin to the DIN pin of the CY7C187 SRAM.

The CMX639 DEC DATA CLK output is used to:

1. Control the timing of encoded (voice) data writes to the SRAM chip.
2. Control the timing of data being passed back to the CMX639 for decoding.
3. Strobe the binary counter ICs to create addresses for SRAM access.

The DEC DATA CLK output is passed through two inverters. The output of the first inverter is connected to the /WE (write enable) pin of the SRAM IC. The output of the second inverter is connected to the 1CLK pin of the first binary counter IC. This configuration is chosen so that the memory address is incremented after the SRAM write has been completed.

The 1CLR and 2CLR inputs of each binary counter IC are tied to V_{SS} so that only the enable inputs (1CLK and 2CLK) control when the counters increment. The two binary counter ICs are cascaded to produce a 16-bit counter whose outputs are connected to the address inputs of the SRAM IC. The SRAM address formed by the cascaded binary counter increments each time the Decoder Data Clock falls from high to low.

The encoded data bit from the CMX639 is latched into the CY7C187 DIN pin when the /WE signal is low. When /WE is high and the address is stable, a data bit appears at the DOUT pin of the CY7C187 and is presented to the DEC INPUT pin of the CMX639. The CMX639 converts the resulting serial data stream from the CY7C187 to an analog signal which is then presented at the DEC OUTPUT pin.

The cascaded binary counter must cycle through its entire range before a data bit that has been written into the memory can be read. The resulting audio delay is given by:

$$\text{Delay} = T \{\text{sec/cycle}\} * 2^N \text{ cycles}$$

Where:

T = period of the CMX639 decoder data clock signal

N = number of bits used in the cascaded binary counter

For example, if all sixteen bits of the counter are used and the decoder data clock frequency is 64kHz, the delay would be:

$$\text{Delay} = 1/64000 * 2^{16} = 1.024 \text{ seconds}$$

If a shorter delay is desired, the two switches connecting the counter outputs and address inputs can be opened. For example, if only 14 bits of the counter are used, the delay is reduced by a factor of four, to 0.256 seconds. The range of delays could be increased even more by adding more switches and by making the sampling frequency adjustable.

4 Conclusion

Two-way radios commonly drop the first few hundred milliseconds of received speech until the incoming CTCSS tone has been detected. A workaround for this problem is to store the voice and delay its transmission until the CTCSS detection time has elapsed. This document presented one method for overcoming this situation. It is hoped that this document will assist engineers who wish to eliminate this behavior from their two-way radio designs.


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