FET Circuit Applications

National Semiconductor
Application Note 32
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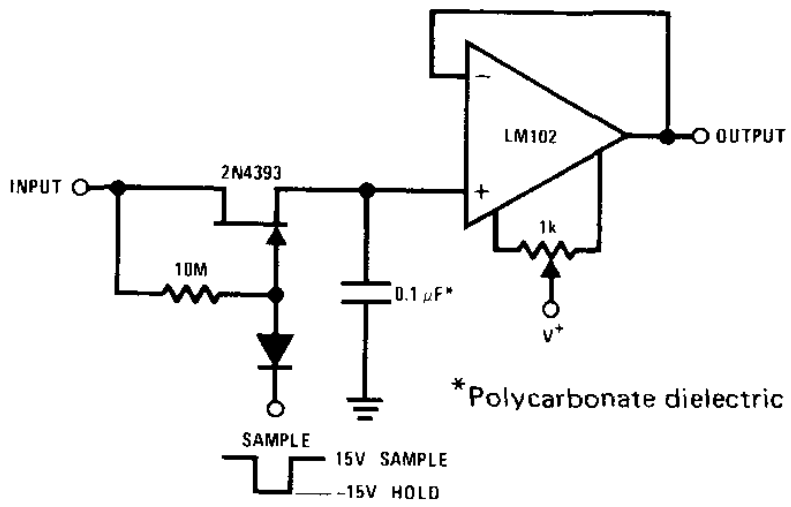
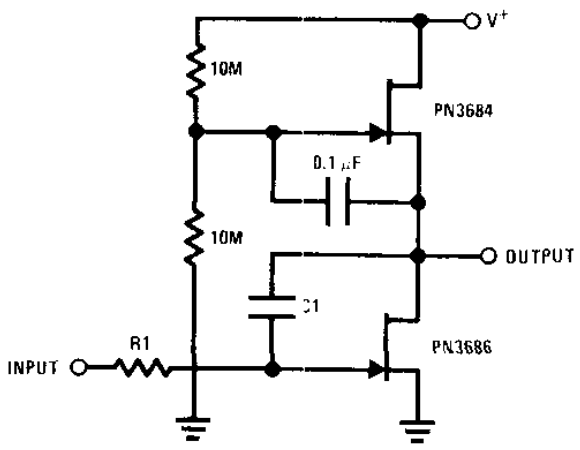


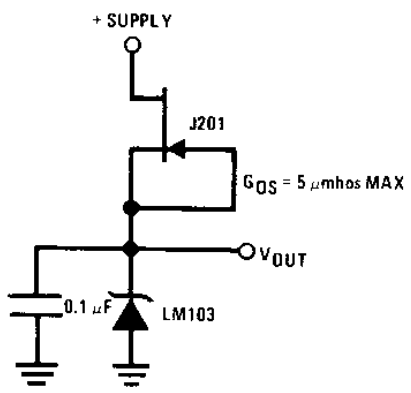
Sample and Hold With Offset Adjustment

The 2N4393 JFET was selected because of its low I_{GSS} (<100 pA), very low $I_{D(OFF)}$ (<100 pA) and low pinchoff voltage. Leakages of this level put the burden of circuit performance on clean, solder-resin free, low leakage circuit layout.



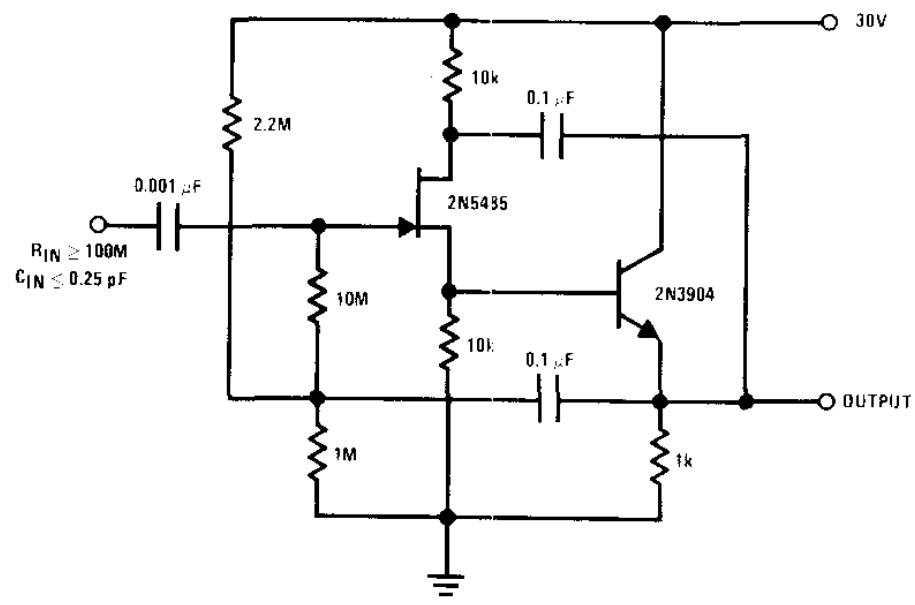
JFET AC Coupled Integrator

This circuit utilizes the "μ-amp" technique to achieve very high voltage gain. Using C1 in the circuit as a Miller integrator, or capacitance multiplier, allows this simple circuit to handle very long time constants.



Low Power Regulator Reference

This simple reference circuit provides a stable voltage reference almost totally free of supply voltage hash. Typical power supply rejection exceeds 100 dB.



Ultra-High Z_{IN} AC Unity Gain Amplifier

Nothing is left to chance in reducing input capacitance. The 2N5485, which has low capacitance in the first place, is operated as a source follower with bootstrapped gate bias resistor and drain.