EECS 240
Analog Integrated Circuits

Topic 13:
Two Stage OTAs

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OTA Realizations

Single stage OTA

- Single high impedance (voltage gain) node
- Near maximum power efficiency
- Limited gain and/or output range
- Can be combined with cascodes, gain boosting
- Examples:
  - Telescopic OTA
    - Maximum power efficiency
    - Limited input common-mode range
  - Folded cascode
    - Large input common-mode range
    - Slightly improved output range
    - Folding adds noise and power penalty

Multi stage OTA

- Advantages over single stage OTA
  - Reduced interaction between gain and output range
  - Somewhat higher drive capability for given C_{in}
- Disadvantages
  - Increased power dissipation or reduced speed
  - Need for compensation
- Examples:
  - Miller-compensated 2-stage OTA
  - OTA with preamp (power efficiency?)
  - Nested Miller compensation

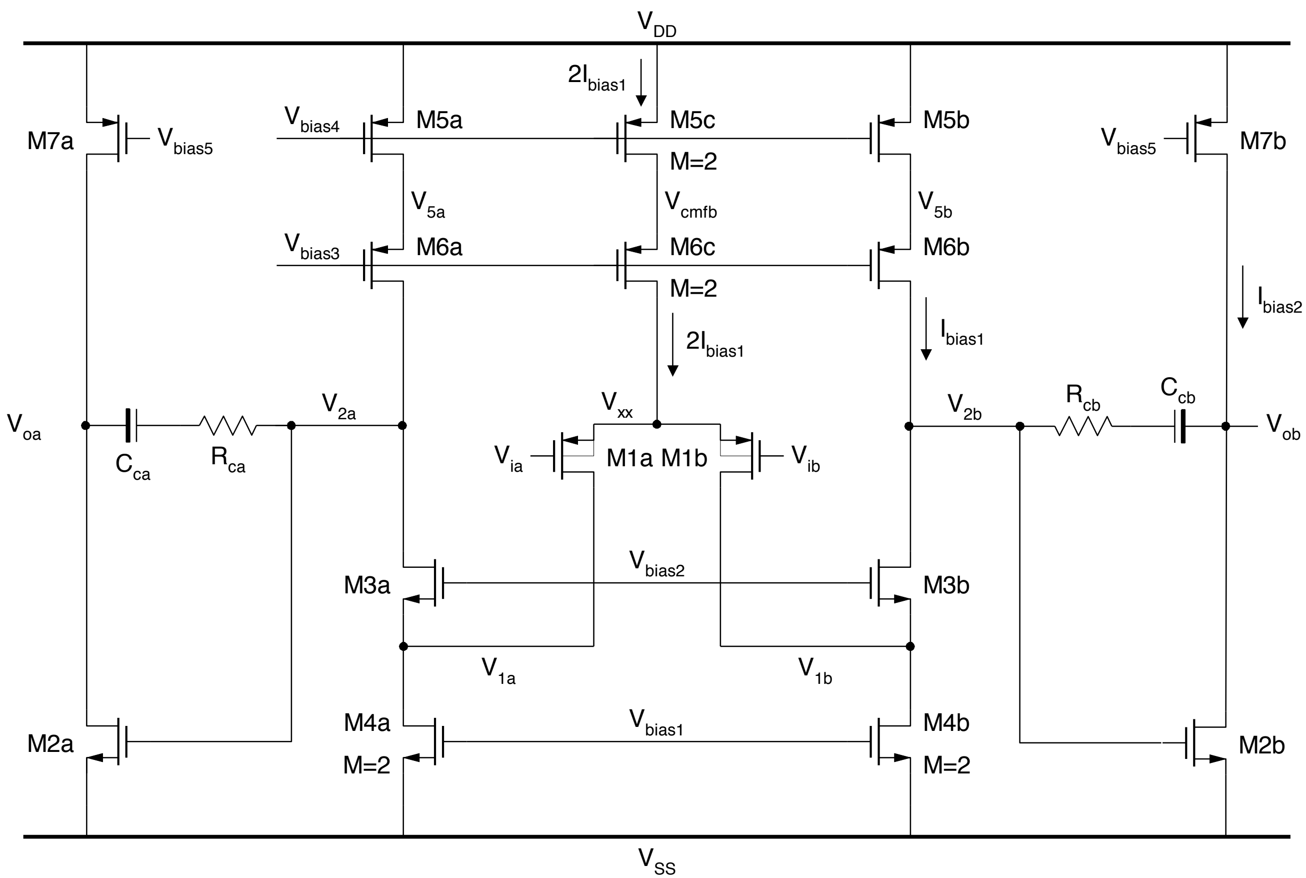
Multi-Stage OTAs

- Advantage
  - Higher gain
  - Improved output voltage swing
  - Potentially reduced input capacitance
  - Power dissipation? Noise?

- Challenges
  - Stability: needs compensation (usually)
  - Reduced bandwidth (2 … 3 times smaller per added stage)

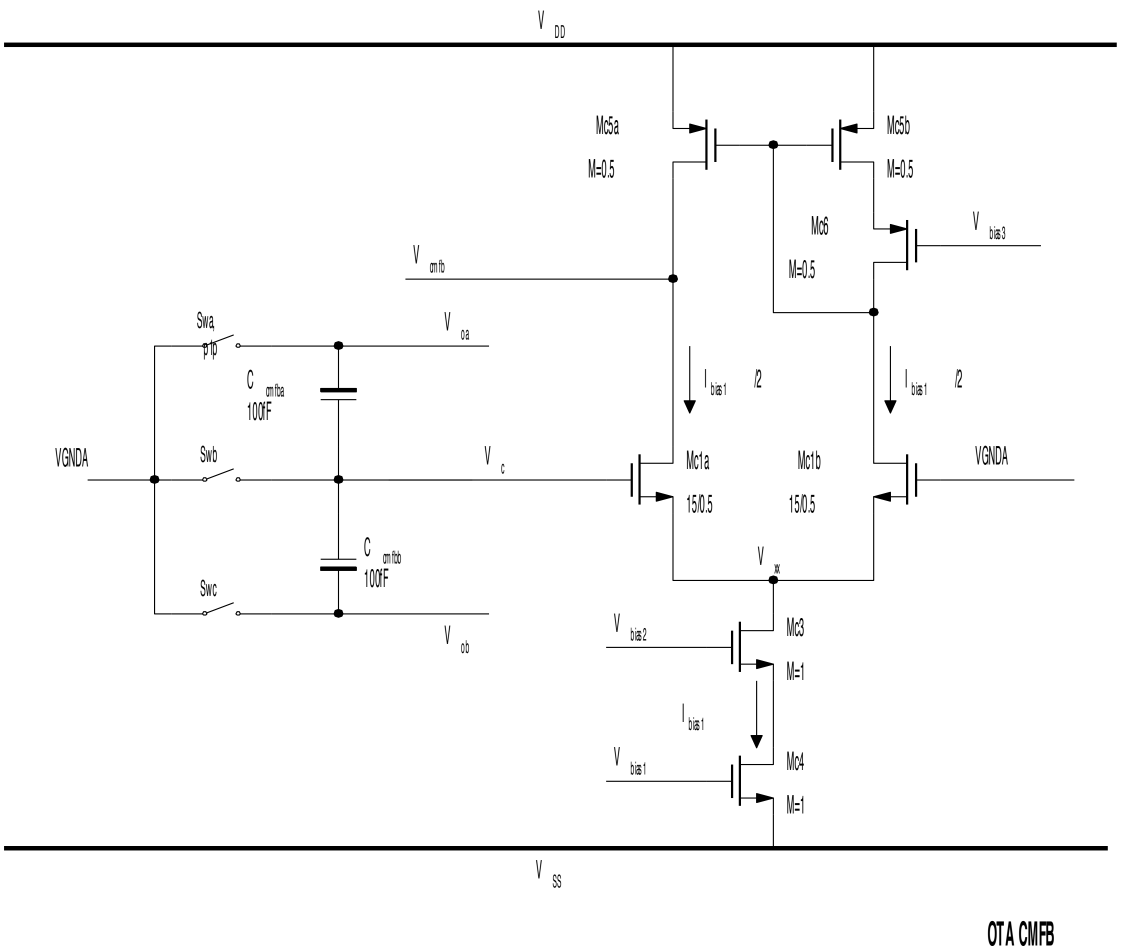
- Approaches
  - 2 high-gain stages with Miller compensation
  - Wide-band preamp (e.g. T. Cho, JSSC 3/95)
  - Nested Miller compensation (e.g. G&M, 4th ed.)

2-Stage OTA Example



OTA Core

2-Stage CMFB



V DD
Mc5a
M=0.5
Mc5b
M=0.5
Mc6
M=0.5
V bias3
V cmfb
Swa, p1p
V oa
C cmfba
100fF
I bias1 /2
I bias1 /2
VGNDA
Swb
V c
Mc1a
15/0.5
Mc1b
15/0.5
VGNDA
C cmfbb
100fF
V xx
Swc
V ob
V bias2
Mc3
M=1
I bias1
V bias1
Mc4
M=1
V SS
OTA CMFB

Compensation Techniques

- Narrowbanding
  - Very small compensated bandwidth
  - Lower dominant pole or add new dominant pole
  - E.g. offset cancellation loop

- Miller compensation
  - Capacitive feedback splits poles
  - Zero adds phase lag
    - Nulling resistor
    - Cascode compensation

No Compensation

$$p_1 = -\frac{1}{R_1 C_1}$$

$$p_2 = -\frac{1}{R_2 C_2} \qquad C_2 = C_L$$

$$a_{v0} = g_{m1} R_1 g_{m2} R_2$$

2 dominant poles →
poor phase margin if placed into feedback loop

Miller Compensation

$$p_1 \approx -\frac{1}{(1+g_{m2}R_2)R_1C_c} \approx -\frac{g_{m1}}{a_{v0}C_c}$$

$$p_2 \approx -\frac{g_{m2}C_c}{C_1C_2 + C_c(C_1+C_2)}$$

$$\approx -\frac{g_{m2}}{C_2} \qquad C_1 << C_c, C_2$$

$$z = +\frac{g_{m2}}{C_c}$$

$$a_{v0} = g_{m1}R_1g_{m2}R_2$$

- RHP zero
- Caused by capacitive feed-forward
- Often adds significant phase lag
  (see root locus)

Phase Margin Engineering

$$\omega_u \approx F \frac{g_{m1}}{C_c}$$

$$|p_2|, z >> \omega_u \quad \text{of } T(s)$$

choose $|p_2| \geq K\omega_u$

$$C_c \geq KFC_2 \frac{g_{m2}}{g_{m1}}$$

- Choose K>2 for reasonable phase margin
- Increasing $C_L=C_2$ *lowers* phase margin

$$\frac{z}{\omega_u} = \underbrace{\frac{1}{F}}_{<1} \underbrace{\frac{g_{m2}}{g_{m1}}}_{1..10 \quad \text{(MOS)}}$$

- Zero adds significant phase lag unless $g_{m2}>>Fg_{m1}$, regardless of C_c

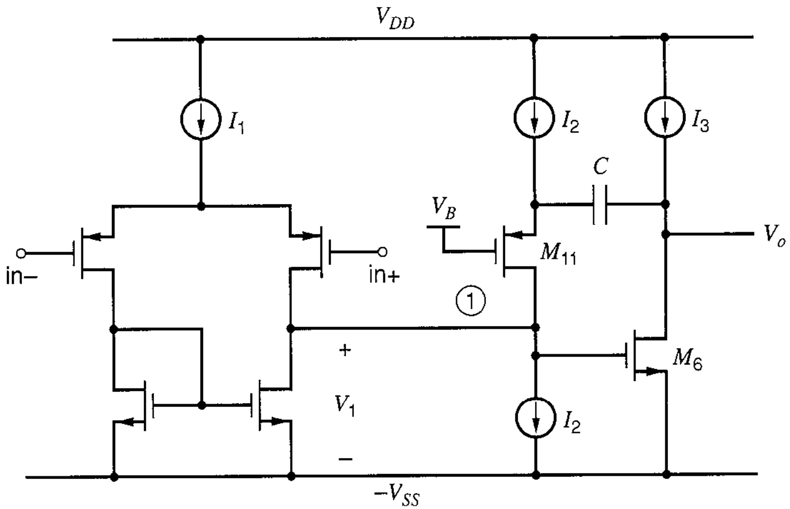
$$\frac{z}{|p_2|} \approx \frac{C_2}{C_c}$$

Mitigating Lag from Zero

- Unilateral Feedback
  - Source Follower
    - Limits output swing
  - Cascode Compensation
    - Ahuja, JSSC 12/1983
    - Ribner, JSSC 12/1984

- Nulling Resistor
  - Zero to infinity
  - Zero cancels p_2

Cascode Compensation (Ahuja)



$$p_1 \approx -\frac{1}{(1+g_{m2}R_2)R_1C_c} \approx -\frac{g_{m1}}{a_{v0}C_c}$$

$$p_2 \approx -\frac{g_{m2}}{C_c+C_2}\frac{C_c}{C_1}$$

$$= p_2^* \underbrace{\frac{C_2}{C_c+C_2}\frac{C_c}{C_1}}_{\text{usually } >1}$$

- No zero (ideal cascode)
- p_2 at higher frequency
- Translates into smaller C_c for given C_2
- Problems:
  - Current I_2
  - Slewing
  - Mismatch (in I_2) causes offset

Cascode Compensation (Ribner)

- Uses cascode in signal path
- No new current path
- Avoids slewing and matching problem
- 3rd order response
  → very difficult to design

Nulling Resistor R_z

$$z \rightarrow \frac{1}{\left(\frac{1}{g_{m2}} - R_Z\right)C_c}$$

$$p_1, p_2 : \quad \text{no change}$$

$$p_3 \approx -\frac{1}{R_z C_1}$$

- R_z limits feedforward current at high frequency
- Zero moves to higher frequency (and ultimately LHP)
- New pole p_3

Zero to Infinity

$$R_z = \frac{1}{g_{m2}}$$

$$z \rightarrow \infty$$

$$p_3 \approx -\frac{g_{m2}}{C_1}$$

$$\omega_u \approx F\frac{g_{m1}}{C_c} \qquad |p_2|,|p_3| >> \omega_u$$

$$\frac{|p_3|}{\omega_u} = \frac{1}{F}\frac{g_{m2}}{g_{m1}}\frac{C_c}{C_1} >> \underbrace{1}_{\text{usually}}$$

For $|p_2| \geq K\omega_u$

$$C_c \geq KFC_2\frac{g_{m1}}{g_{m2}}$$

$$C_2 \leq \frac{C_c}{KF}\frac{g_{m2}}{g_{m1}}$$

- No phase shift from zero
- Phase lag from p_3 decreases as C_c is increased
- Implementation of R_z?

Zero Cancels p_2

$$R_z = \frac{1}{g_{m2}}\left(1 + \frac{C_2}{C_c}\right)$$

$$p_3 \approx -\frac{1}{R_z C_1}$$ is the new nondominant pole

$$\omega_u \approx F\frac{g_{m1}}{C_c} \qquad |p_3| >> \omega_u$$

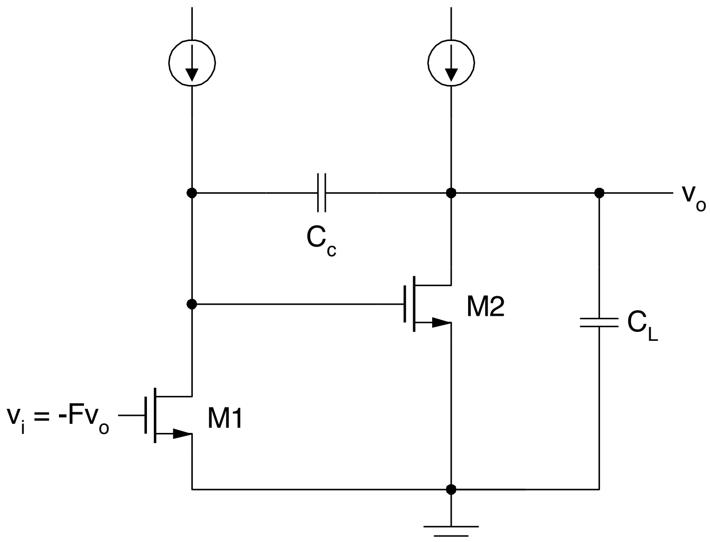
For $|p_3| \geq K\omega_u$

$$C_2 \leq \frac{C_c}{KF}\frac{g_{m2}}{g_{m1}}\frac{C_c}{C_1}$$

- Increased bandwidth
- Smaller C_c for given C_2
- Doublet → not necessarily faster settling

Noise Analysis

Simplified schematic:



$$sC_c(v_x - v_o) - Fg_{m1}v_o + i_{n1} = 0$$

$$g_{m2}v_x + v_o s(C_L + C_c) + i_{n2} = 0$$

ERROR: 2nd Equation misses $v_x C_c$ term

→

$$v_o = \frac{1}{Fg_{m1}} \frac{1}{1 + \frac{s}{\omega_o Q} + \frac{s^2}{\omega_o^2}} \left(i_{n1} - i_{n2} \frac{sC_c}{g_{m2}} \right)$$

with

$$\omega_o^2 = \frac{Fg_{m1}g_{m2}}{C_c(C_c + C_L)}$$

$$\omega_o Q = \frac{Fg_{m1}}{C_c}$$

Total Noise at Output

$$\overline{v_{oT}^2} = \frac{k_B T}{C_c}\frac{\gamma}{F}\left(1 + \underbrace{\frac{FC_c}{C_c + C_L}}_{<1\ \text{(noise from M2)}}\right)$$

- Noise from first stage dominates
- Noise capacitor: C_c, NOT C_L!

Nested Miller Compensation

- >2 gain stages
- Higher order response presents design challenge
- Not (yet?) used much

Ref: R. G. H. Eschauzier and J. H. Huijsing. *Frequency Compensation Techniques for Low-Power Operational Amplifiers.* Kluwer, 1995.

J. Huijsing. *Operational Amplifiers, Theory and Design*. Kluwer, 2001.