

S/PDIF Interface Board user guide

By Ian Jin and George Richardson Ver. 1.0

Description

The S/PDIF Interface Board was designed to mate with the I2S FIFO KIT to add S/PDIF receiving and transmitting capability. By integrating with the I2S FIFO KIT and the clock board, we can create an S/PDIF FIFO, an I2S FIFO with S/PDIF receiver, or an S/PDIF FIFO with I2S output.

The S/PDIF Interface Board uses TI/BB's most up to date 216 KHz DIX9211 for the S/PDIF receiver and transmitter. The DIX9211 was tested and found to be very stable throughout the full S/PDIF working range from 44.1 KHz to 192 KHz. In addition, the chip's internal DIR and DIT are totally independent from each other which is required for the FIFO's asynchronous architecture.

In order to improve the signal quality and to reduce additive transmission jitter, the S/PDIF Interface Board is equipped with a re-clock circuit, a low jitter dedicated clock fan-out buffer and an enhanced power supply.

Based on the open concept, sockets for the digital transformers are provided for future customized upgrades.

KIT includings

- An assembled and tested S/PDIF Interface Board (Pb free SMT)
- Two 5" double-ended PH 2.0mm 7-pin I2S cables
- One 6" double-ended U.FL coaxial cable for MCLK output
- One 2" 10-pin FPC/FFC cable to interface with the I2S FIFO Board
- Two BNC to RCA adapters

Features and specifications

- S/PDIF input and output range: 44.1 KHz 16-bit to 192 KHz 24-bit
- Three S/PDIF inputs:
 - Coaxial: BNC 75 ohm
 - Optical: Toslink
 - TTL: 2-pin connector LVTTL (3.3V) with 5V tolerance
- Three S/PDIF outputs
 - Coaxial: BNC 75 ohm
 - Balanced: AES/EBU XLR 110 ohm
 - Optical: Toslink
- 216 KHz TI/BB DIX9211 digital audio interface featuring internally independent DIR and DIT
- Low jitter S/PDIF coaxial and XLR drivers to provide better phase noise performance
- I2S input
 - LVTTL (3.3V) logic input level
 - 44.1 KHz, 48 KHz, 88.2 KHz, 96 KHz, 176.4 KHz, 192 KHz – 16- or 24- bit
 - 7-pin PH 2.0mm connector, or
 - Three 50 ohm U.FL coaxial connectors
- I2S output
 - LVTTL (3.3V) logic output level
 - 44.1 KHz, 48 KHz, 88.2 KHz, 96 KHz, 176.4 KHz, 192 KHz – 16- or 24- bit
 - 7-pin PH 2.0mm connector, and
 - Three 50 ohm U.FL coaxial connectors
- MCLK input
 - LVTTL (3.3V) logic output level
 - 128*Fs, 256*Fs (default) or 512*Fs

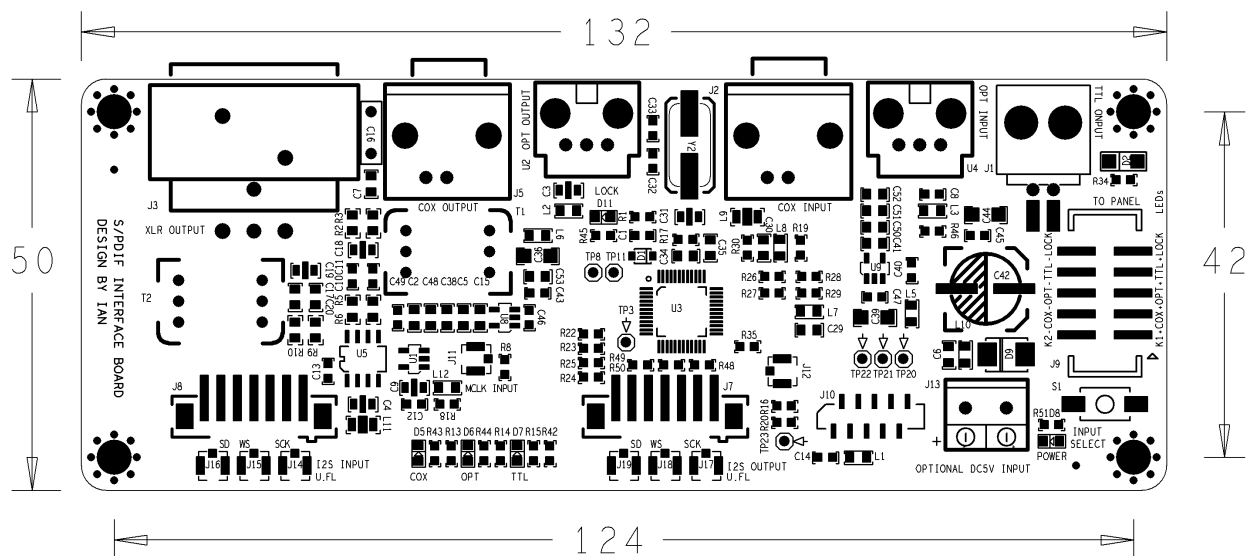
50 ohm U.FL coaxial input connector

- S/PDIF signal is re-clocked by the MCLK before sending to the driver
- On board digital audio transformer sockets to facilitate future upgrading
- LED indicators for power, lock and input selections
- On board push button for S/PDIF source selection
- Header is provided for an external control panel
- Power supply

On-board 9 μ V RMS low-noise, high-PSRR LDOs

Enhanced high performance EMI filters

Layout and dimensions (in mm)



Connectors and jumpers on the S/PDIF Interface Board

- S/PDIF inputs:

J2: 75 ohm BNC connector for coaxial S/PDIF input

U4: Toslink receiver for optical S/PDIF input

J1: 2-pin 2.54mm connector for TTL S/PDIF input

- S/PDIF outputs:

J5: 75 ohm BNC connector for coaxial S/PDIF output

J2: 110 ohm XLR connector for balanced AES/EBU output

U2: Toslink transmitter for optical S/PDIF output

- I2S output from DIR:

J7: PH 2.0mm 7-pin connector, configured as

1	2	3	4	5	6	7
GND	SCK	GND	WS	GND	SD	GND

and, U.FL coaxial cable connectors, configured as

J17	J18	J19
SCK	WS	SD

- I2S input to DIT:

J6: PH 2.0 mm 7-pin connector, configured as

1	2	3	4	5	6	7
GND	SCK	GND	WS	GND	SD	GND

or, U.FL coaxial cable connectors, configured as

J14	J15	J16
SCK	WS	SD

- MCLK input to DIT: J11, U.FL coaxial cable connector

- Optional MCLK output from DIR: J12 (NC)

- Digital transformer socket for S/PDIF coaxial output: T1

- Digital transformer socket for AES/EBU XLR output: T2

- Digital audio input source selection button: S1 OPT (default) → COX → TTL → ...(loop back)

- External control panel interface: J9, 10-pin 2.54mm double row header, configured as

Selecting button	COX input LED	OPT input LED	TTL input LED	S/PDIF locked LED
1 - 2	3(+) – 4(-)	5(+) – 6(-)	7(+) – 8(-)	9(+) – 10(-)

- Optional DC input: J13 (do not use if interfaced with the I2S FIFO KIT board)

LED indicators

- S/SPDIF input indicators

D5: COX

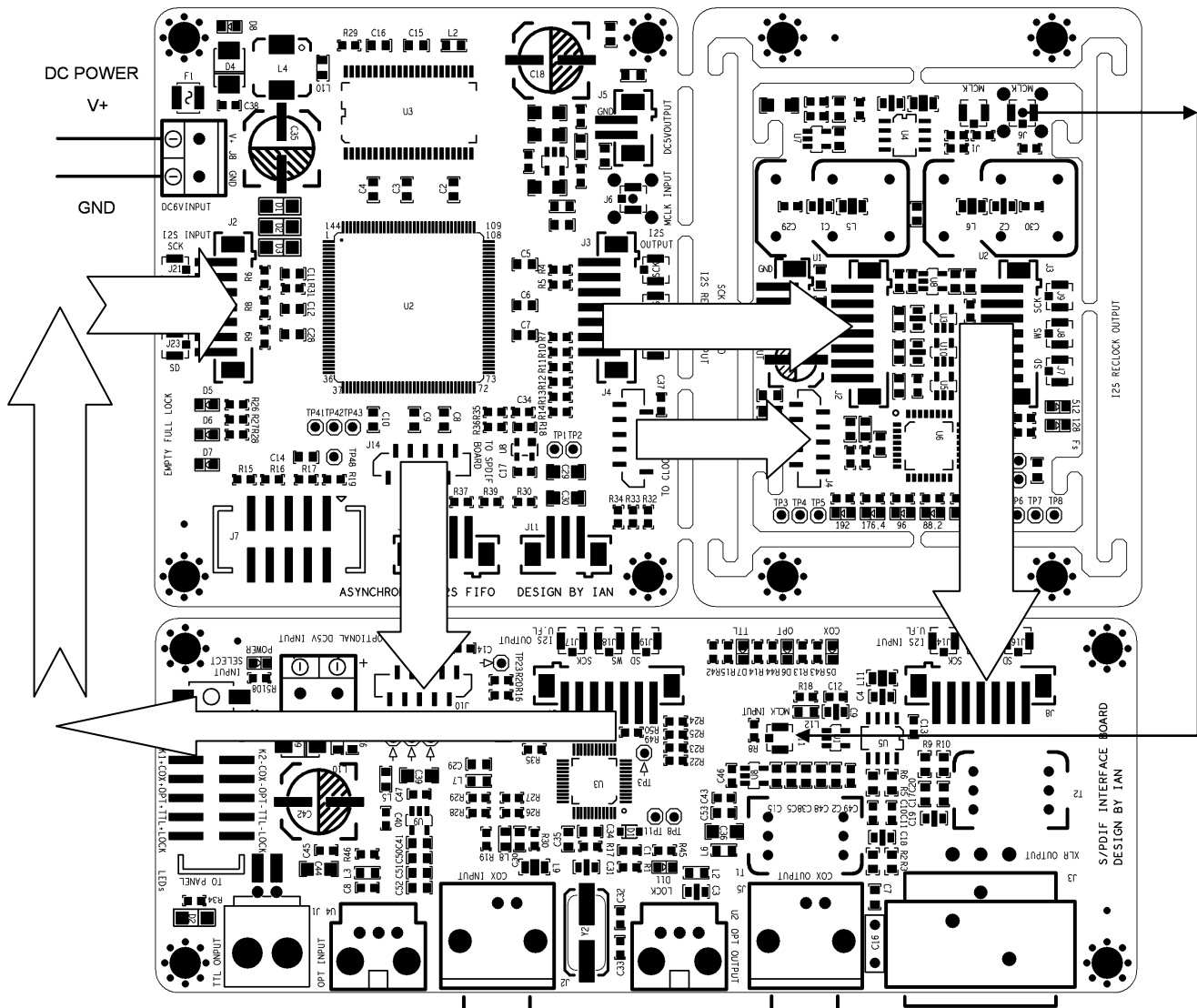
D6: OPT (default)

D7: TTL

- S/SPDIF signal locked indicator:

D11 - Power indicator: D8

How to configure an S/SPDIF FIFO using the I2S FIFO KIT



1. Connect J14 on the I2S FIFO KIT board to J10 on the S/PDIF board with the 10-pin FFC/FPC cable (the connectors are doubled-sided, so the cable can face up or down).
2. Connect the I2S signals from the DIR output to the FIFO input. This can be done either with the double-ended 7-pin PH 2.0mm cable from J7 on the S/PDIF board to J2 on the I2S FIFO KIT board, or by three U.FL coaxial cables

	S/PDIF Board → I2S FIFO KIT board
SCK	J17 → J21
WS	J18 → J22
SD	J19 → J23

3. Connect the I2S signals from the clock board re-clocked output (or from the I2S FIFO KIT board) to the DIT input. This can be done with either the double-ended 7-pin PH 2.0mm cable from J3 on the Dual XO Clock board (or the corresponding port on the I2S FIFO Board or other clock board) to J8 on the S/PDIF Board, or by three U.FL coaxial cables (connecting to the Dual XO clock board for example)

	S/PDIF Interface Board ← Dual XO Clock board
SCK	J14 ← J9
WS	J15 ← J8
SD	J16 ← J7

4. Connect MCLK output from the clock board to the DIT input on the S/PDIF board with the U.FL coaxial cable J1 or J6 on the Dual XO Clock Board (or corresponding MCLK output from another clock board) to J11 on the S/PDIF board.
5. For other connections, please refer to the user's manual for the I2S FIFO KIT or the user's manual for the clock board for more details.

How to configure an I2S FIFO with S/PDIF digital audio receiver

In this configuration, only the DIR section of the S/PDIF Board is used. The DIT section is not connected. The connections are the same as for an S/PDIF FIFO, except (i) the MCLK input and I2S input on the S/PDIF board are left open and (ii) the MCLK output and re-clocked I2S output signals from the clock board must be connected to the DAC or DSP.

How to configure an S/PDIF FIFO with I2S output

In this configuration, we setup an S/PDIF FIFO, and at same time having the I2S output function.

Make the same connections as for an S/PDIF FIFO by integrating the I2S FIFO KIT with the S/PDIF Interface Board.

Then connect the left I2S output port on the clock board (using the 7-pin PH 2.0mm cable or U.FL coaxial cables, whichever is available) to the DAC, as well as the left MCLK output port using the U.FL coaxial cable.

Application notes and tips

- Digital transformer selection

For an S/PDIF FIFO, the digital transformer will influence the sound (although not as much as the clock oscillator does). The board is supplied with a Pulse PE-65612 transformer, which works well for most applications. The Newava Technology S22160 was tested and found to be a good alternative for the coaxial S/PDIF output, while the Scientific Conversion SC947-02 worked well for the XLR AES/EBU output. You are encouraged to try different transformers and decide for yourself.

If the AES/EBU XLR output is not used, it is recommended not to populate the digital transformer socket, T2.

- A U.FL tool is recommended to un-plug the U.FL cables, otherwise the connector and the head of the cable can be damaged when disconnecting the cable.

It is available here: <http://search.digikey.com/us/en/products/U.FL-LP-N-2/H9159-ND/513008>

or you can make your own.

Reference

IEC 60958-3: Digital audio interface - Part 3: Consumer applications

IEC 60958 and **EIAJ CO-1201** cover both consumer and professional definitions

Appendix: picture of a S/PDIF FIFO sample hookup

