

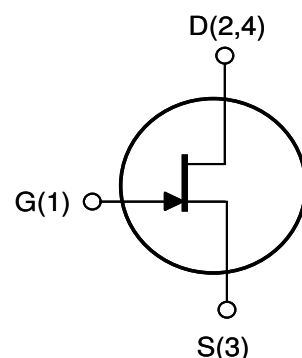
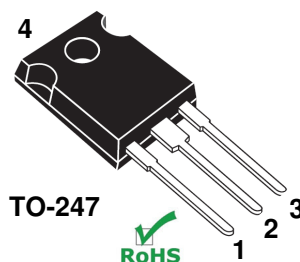
Normally-OFF Trench Silicon Carbide Power JFET

Features:

- Compatible with Standard Gate Driver ICs
- Positive Temperature Coefficient for Ease of Paralleling
- Extremely Fast Switching with No "Tail" Current at 150 °C
- 150 °C Maximum Operating Temperature
- $R_{DS(on)max}$ of 0.100 Ω
- Voltage Controlled
- Low Gate Charge
- Low Intrinsic Capacitance

Applications:

- Solar Inverter
- SMPS
- Power Factor Correction
- Induction Heating
- UPS
- Motor Drive



Internal Schematic

MAXIMUM RATINGS

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current	$I_D, T_j=100$	$T_j = 100\text{ }^\circ\text{C}$	17	A
	$I_D, T_j=150$	$T_j = 150\text{ }^\circ\text{C}$	10	
Pulsed Drain Current ⁽¹⁾	I_{DM}	$T_j = 25\text{ }^\circ\text{C}$	30	A
Short Circuit Withstand Time	t_{SC}	$V_{DD} < 800\text{ V}, T_C < 125\text{ }^\circ\text{C}$	50	μs
Power Dissipation	P_D	$T_C = 25\text{ }^\circ\text{C}$	114	W
Gate-Source Voltage	V_{GS}	AC ⁽²⁾	-15 to +15	V
Operating and Storage Temperature	T_j, T_{stg}		-55 to +150	$^\circ\text{C}$
Lead Temperature for Soldering	T_{sld}	1/8" from case < 10 s	260	$^\circ\text{C}$

⁽¹⁾ Limited by pulse width

⁽²⁾ $R_{gEXT} = 1\text{ }\Omega$, $t_p \leq 200\text{ ns}$, see Figure 6 for static conditions

THERMAL CHARACTERISTICS

Parameter	Symbol	Value		Unit
		Typ	Max	
Thermal Resistance, junction-to-case	R_{thJC}	-	1.1	$^\circ\text{C} / \text{W}$
Thermal Resistance, junction-to-ambient	R_{thJA}	-	50	

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	

Off Characteristics

Drain-Source Blocking Voltage	BV_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 600 \mu\text{A}$	1200	-	-	V
Total Drain Leakage Current	I_{DSS}	$V_{DS} = 1200 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_j = 25^\circ\text{C}$	-	100	600	μA
		$V_{DS} = 1200 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_j = 150^\circ\text{C}$	-	300	-	
		$V_{DS} = 1200 \text{ V}$, $V_{GS} \leq -15 \text{ V}$, $T_j = 25^\circ\text{C}$	-	1	-	
		$V_{DS} = 1200 \text{ V}$, $V_{GS} \leq -15 \text{ V}$, $T_j = 150^\circ\text{C}$	-	10	-	
Total Gate Reverse Leakage	I_{GSS}	$V_{GS} = -15 \text{ V}$, $V_{DS} = 0 \text{ V}$	-	-0.1	-0.3	mA
		$V_{GS} = -15 \text{ V}$, $V_{DS} = 1200 \text{ V}$	-	-0.1	-	

On Characteristics

Drain-Source On-resistance	$R_{DS(on)}$	$I_D = 10 \text{ A}$, $V_{GS} = 3 \text{ V}$, $T_j = 25^\circ\text{C}$	-	0.08	0.1	Ω
		$I_D = 10 \text{ A}$, $V_{GS} = 3 \text{ V}$, $T_j = 100^\circ\text{C}$	-	0.2	-	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = 1 \text{ V}$, $I_D = 34 \text{ mA}$	0.75	1.00	1.25	V
Gate Forward Current	I_{GFWD}	$V_{GS} = 3 \text{ V}$	-	220	-	mA
Gate Resistance	R_G	$f = 1 \text{ MHz}$, drain-source shorted	-	6	-	Ω
	$R_{G(ON)}$	$V_{GS} > 2.7 \text{ V}$; See Figure 6	-	0.5	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{DD} = 100 \text{ V}$	-	670	-	pF
Output Capacitance	C_{oss}		-	103	-	
Reverse Transfer Capacitance	C_{rss}		-	97	-	
Effective Output Capacitance, energy related	$C_{o(er)}$	$V_{DS} = 0 \text{ V to } 600 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	60	-	

Switching Characteristics

Turn-on Delay	t_{on}	$V_{DS} = 600 \text{ V}$, $I_D = 12 \text{ A}$, Inductive Load, $T_j = 25^\circ\text{C}$ Gate Driver = +15 V, -15 V,	-	10	-	ns
Rise Time	t_r		-	12	-	
Turn-off Delay	t_{off}		-	30	-	
Fall Time	t_f		-	25	-	
Turn-on Energy	E_{on}	See Figure 17 and application note for gate drive recommendations	-	68	-	μJ
Turn-off Energy	E_{off}		-	87	-	
Total Switching Energy	E_{ts}		-	155	-	
Turn-on Delay	t_{on}	$V_{DS} = 600 \text{ V}$, $I_D = 12 \text{ A}$, Inductive Load, $T_j = 150^\circ\text{C}$ Gate Driver = +15 V, -15 V,	-	10	-	ns
Rise Time	t_r		-	15	-	
Turn-off Delay	t_{off}		-	30	-	
Fall Time	t_f		-	25	-	
Turn-on Energy	E_{on}	See Figure 17 and application note for gate drive recommendations	-	82	-	μJ
Turn-off Energy	E_{off}		-	94	-	
Total Switching Energy	E_{ts}		-	176	-	
Total Gate Charge	Q_g	$V_{DS} = 600 \text{ V}$, $I_D = 5 \text{ A}$, $V_{GS} = +2.5 \text{ V}$	-	30	-	nC
Gate-Source Charge	Q_{gs}		-	1	-	
Gate-Drain Charge	Q_{gd}		-	24	-	

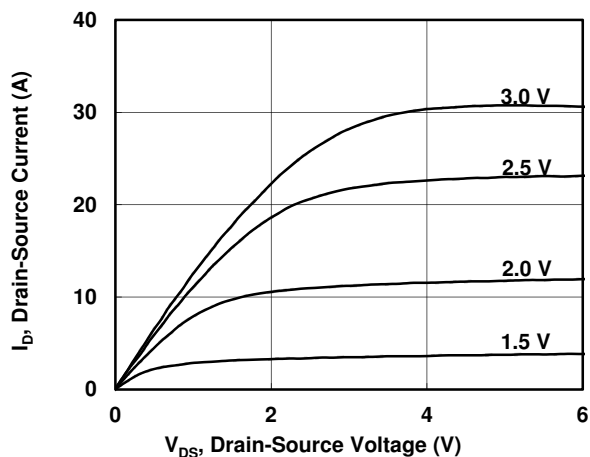
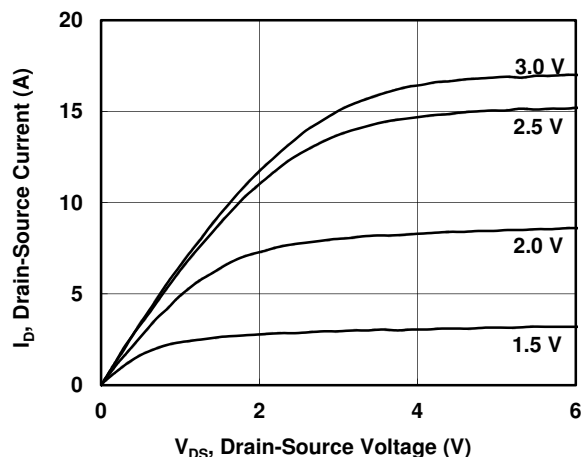
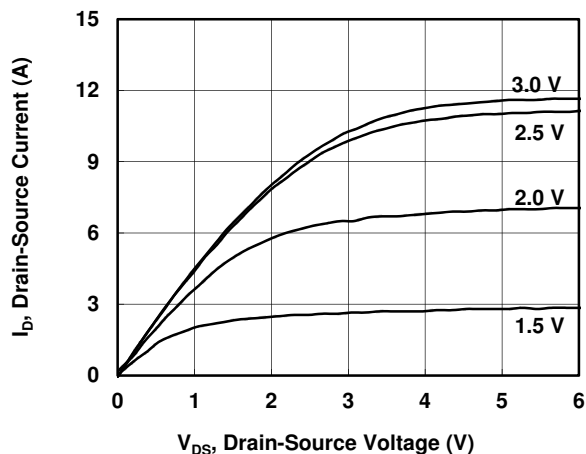
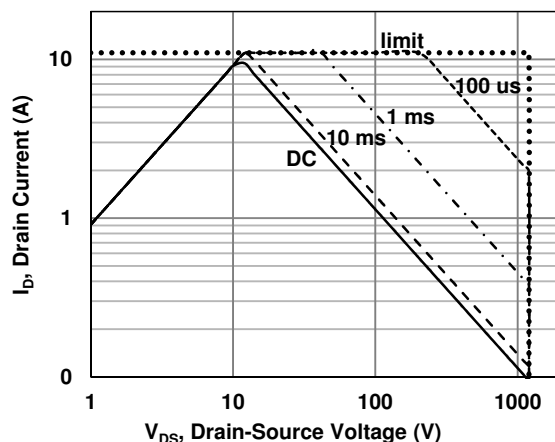
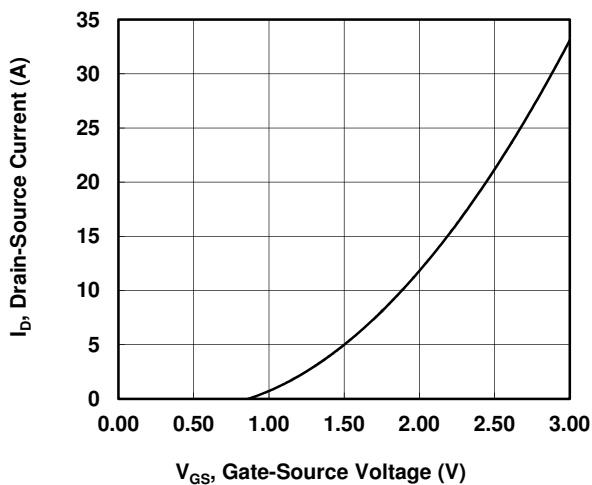
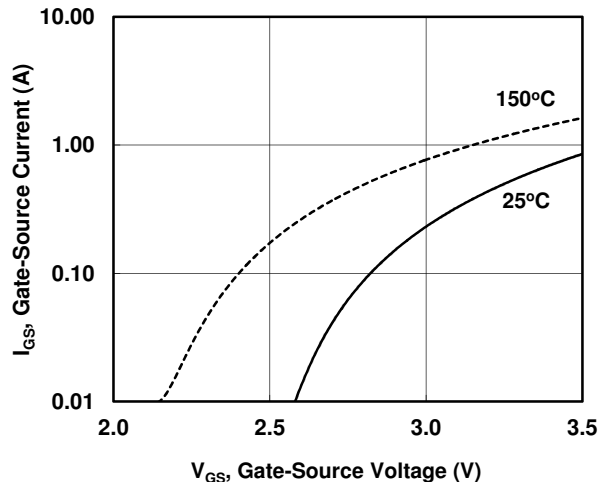
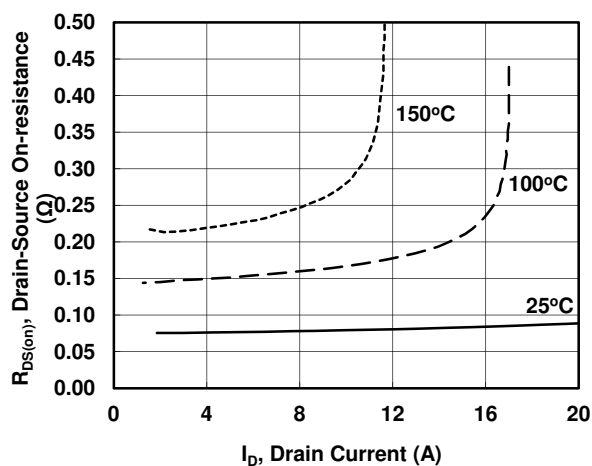
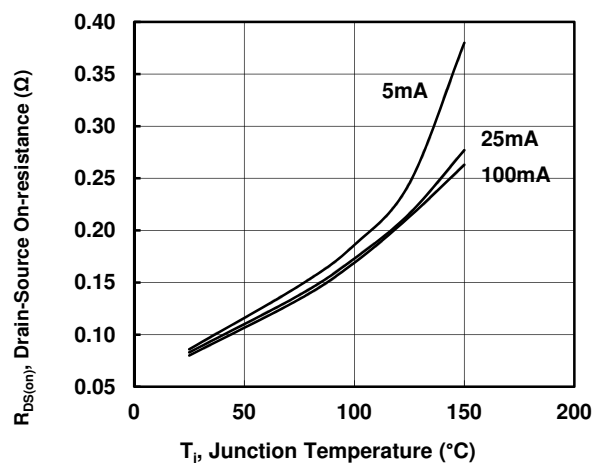
Figure 1. Typical Output Characteristics
 $I_D = f(V_{DS}); T_J = 25\text{ }^\circ\text{C}; \text{parameter: } V_{GS}$

Figure 2. Typical Output Characteristics
 $I_D = f(V_{DS}); T_J = 100\text{ }^\circ\text{C}; \text{parameter: } V_{GS}$

Figure 3. Typical Output Characteristics
 $I_D = f(V_{DS}); T_J = 150\text{ }^\circ\text{C}; \text{parameter: } V_{GS}$

Figure 4. Safe Operating Area
 $I_D = f(V_{DS}); T_C = 25\text{ }^\circ\text{C}, D = 0, \text{parameter: } t_p$

Figure 5. Typical Transfer Characteristics
 $I_D = f(V_{GS}); V_{DS} = 5\text{ V}$

Figure 6. Gate-Source Current
 $I_{GS} = f(V_{GS}); \text{parameter: } T_J$


Figure 7. Drain-Source On-resistance

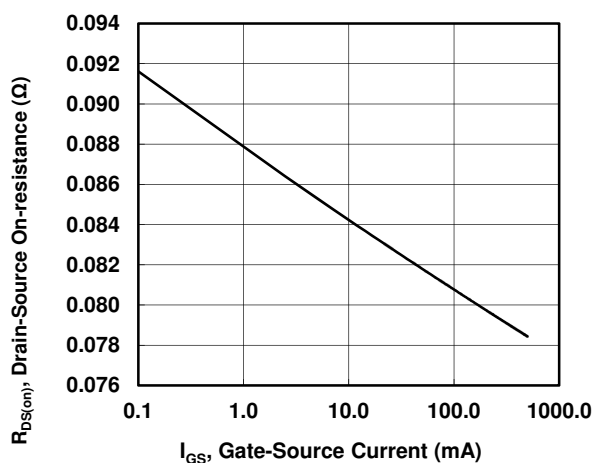
$$R_{DS(on)} = f(I_D); V_{GS} = 3.0 \text{ V}; \text{parameter: } T_j$$


Figure 8. Drain-Source On-resistance

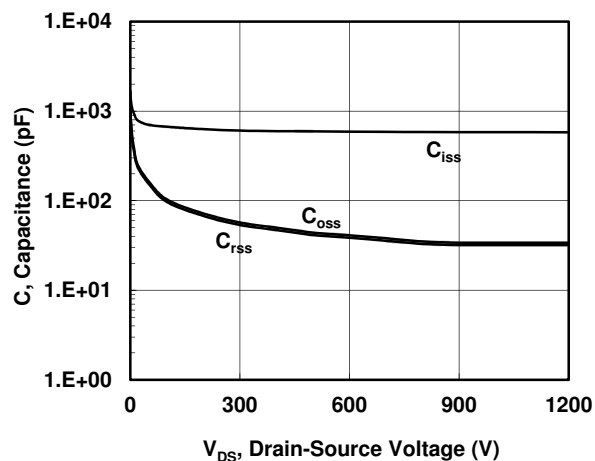
$$R_{DS(on)} = f(T_j); I_D = 10 \text{ A}; \text{parameter: } I_{GS}$$


Figure 9. Drain-Source On-resistance

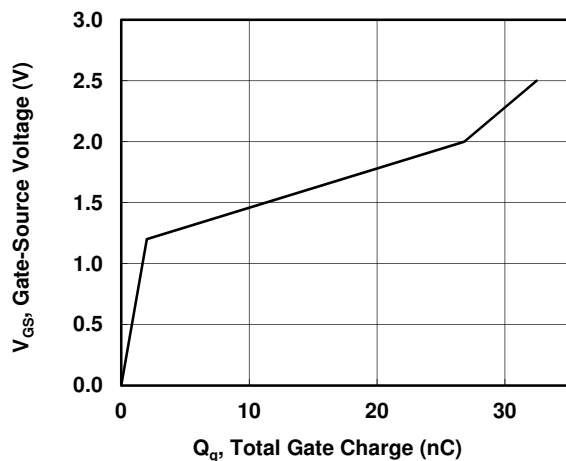
$$R_{DS(on)} = f(I_{GS}); I_D = 10 \text{ A}; T_j = 25^\circ\text{C}$$


Figure 10. Typical Capacitance

$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$


Figure 11. Gate Charge

$$Q_g = f(V_{GS}); V_{DS} = 600 \text{ V}; I_D = 5 \text{ A}; T_j = 25^\circ\text{C}$$


Figure 12. Gate Threshold Voltage

$$V_{th} = f(T_j)$$

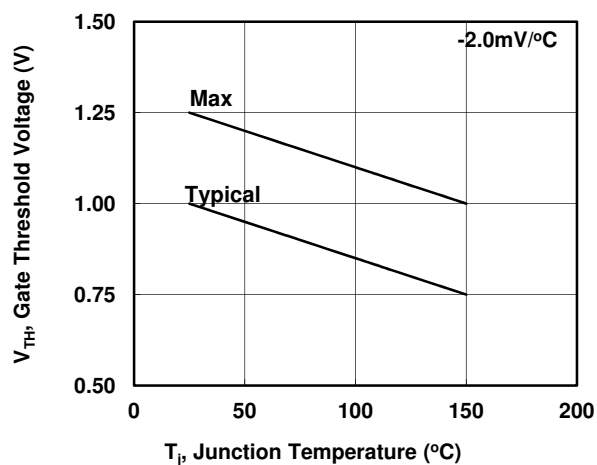
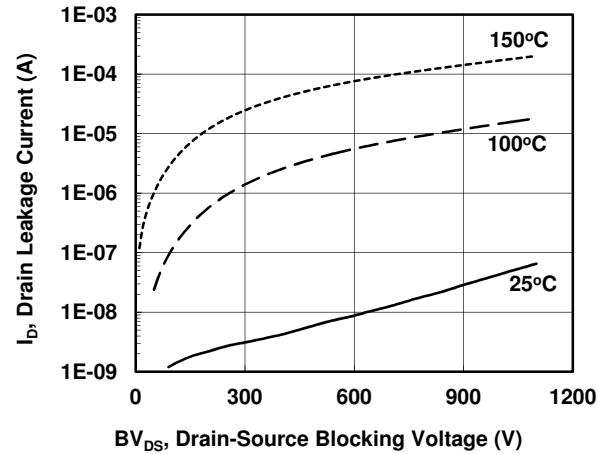


Figure 13. Drain-Source Leakage

$$I_D = f(V_{DS}); V_{GS} = 0 \text{ V}; \text{ parameter: } T_j$$


Figure 14. Transient Thermal Impedance

$$Z_{th(jc)} = f(t_p); \text{ parameter: Duty Ratio}$$

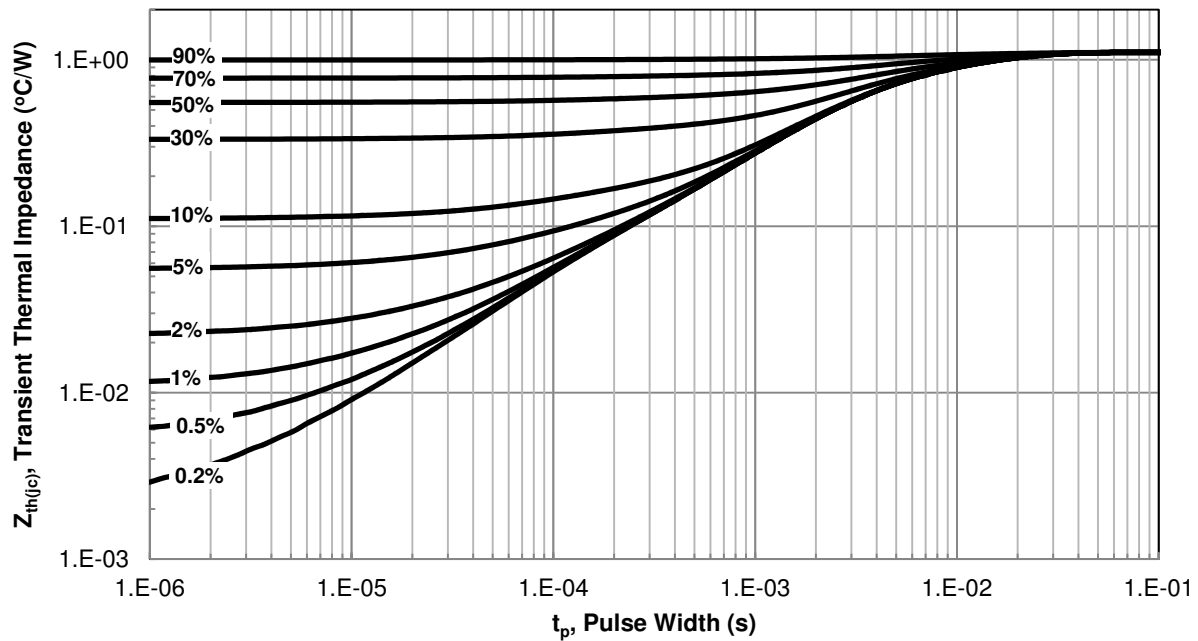
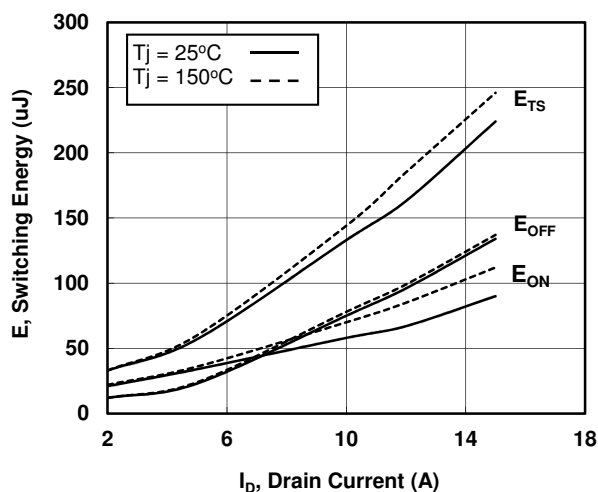
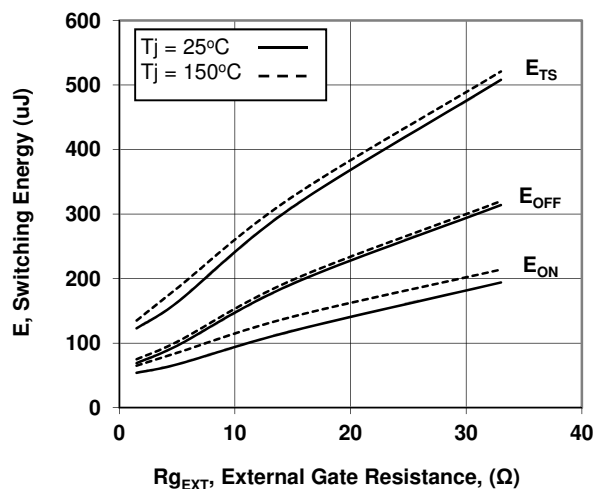
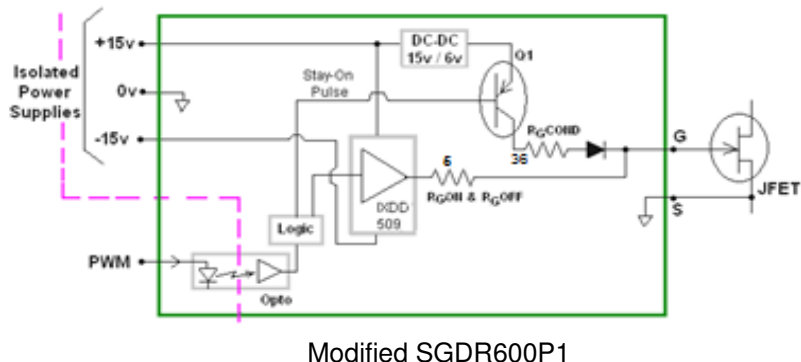
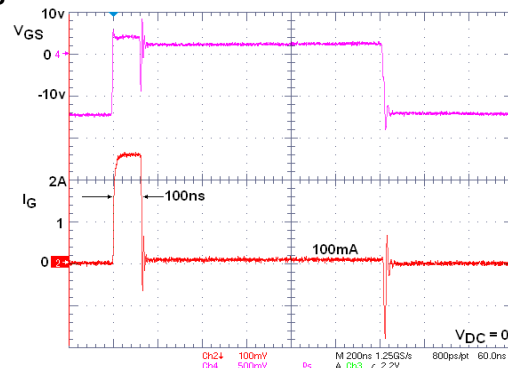
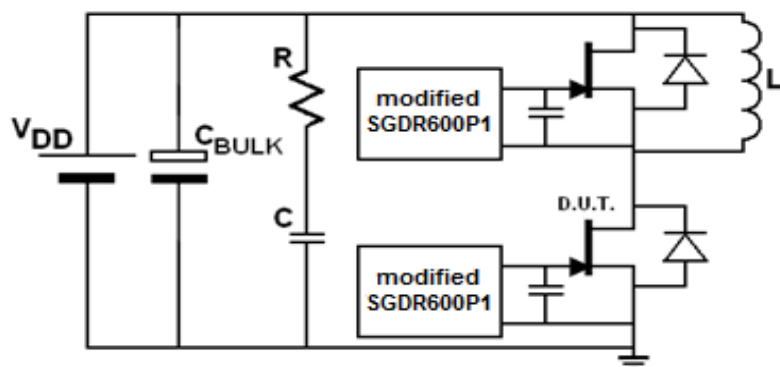


Figure 15. Switching Energy Losses
 $E_s = f(I_D); V_{DS} = 600 \text{ V}; GD = +15 \text{ V}/-15 \text{ V}, R_{GEXT} = 5 \Omega$

Figure 16. Switching Energy Losses
 $E_s = f(R_{GEXT}); V_{DS} = 600 \text{ V}; I_D = 12 \text{ A}, GD = +15 \text{ V}/-15 \text{ V}$

Figure 17. Gate Driver & Switching Test Circuit


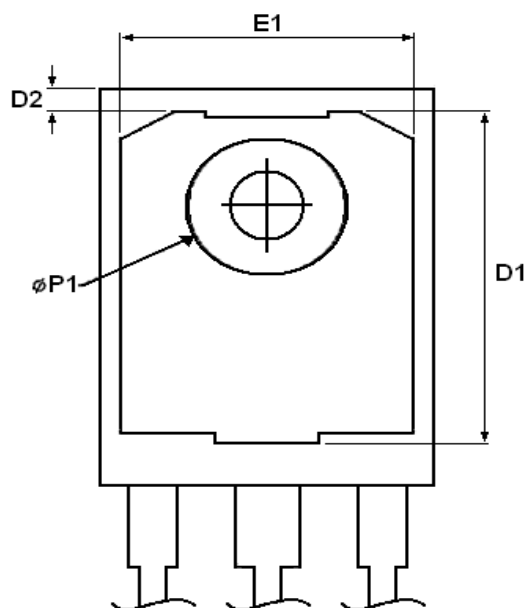
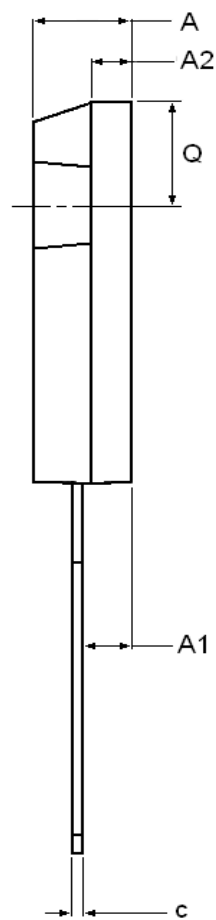
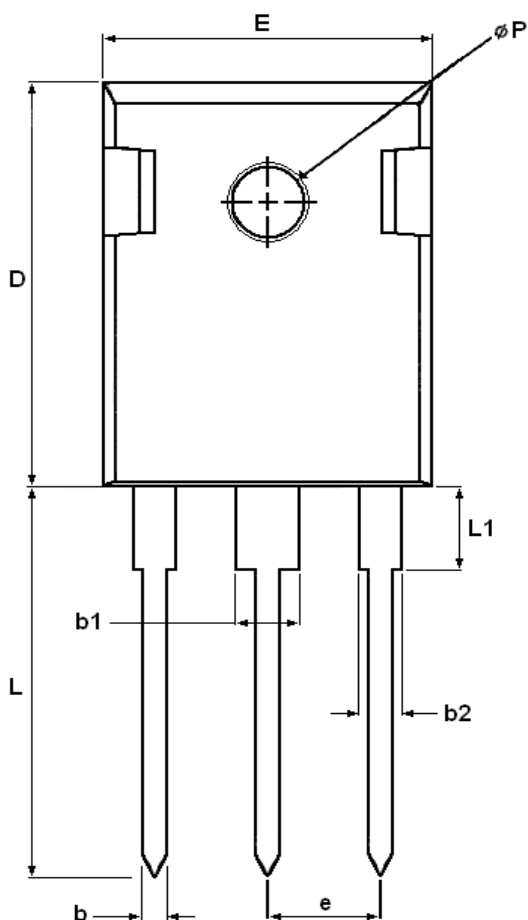
Modified SGDR600P1


Figure 18. Test Circuit & Test Conditions


Test Conditions

- Single Device configuration
- $V_{DD} = 600 \text{ V}$, $I_{LPK} = 12 \text{ A}$, $T_A = 25^\circ\text{C}$
- RC snubber: $R = 22 \Omega$ and $C = 4.7 \text{ nF}$
- $400 \mu\text{H}$ load inductance
- Each device driven by separate modified SGDR600P1
- Gate driver approx. 5mm from gate terminal
- 3.3 nF gate-source capacitive clamp

The SGDR600P1 is a gate driver reference design available for purchase from SemiSouth. See applications note AN-SS3 for full circuit description, test results, schematics, and bill of materials. Gerber files also available upon request.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.903	5.157	0.193	0.203
A1	2.273	2.527	0.090	0.100
A2	1.853	2.108	0.073	0.083
b	1.073	1.327	0.042	0.052
b1	2.873	3.381	0.113	0.133
b2	1.903	2.386	0.042	0.052
c	0.600	0.752	0.024	0.029
D	20.823	21.077	0.820	0.830
D1	17.393	17.647	0.685	0.695
D2	1.063	1.317	0.042	0.052
e	5.450		0.215	
E	15.773	16.027	0.621	0.631
E1	13.893	14.147	0.547	0.557
L	20.053	20.307	0.789	0.799
L1	4.168	4.472	0.165	0.175
Q	6.043	6.297	0.238	0.248
ØP	3.560	3.660	0.140	0.144
ØP1	7.063	7.317	0.278	0.288

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