

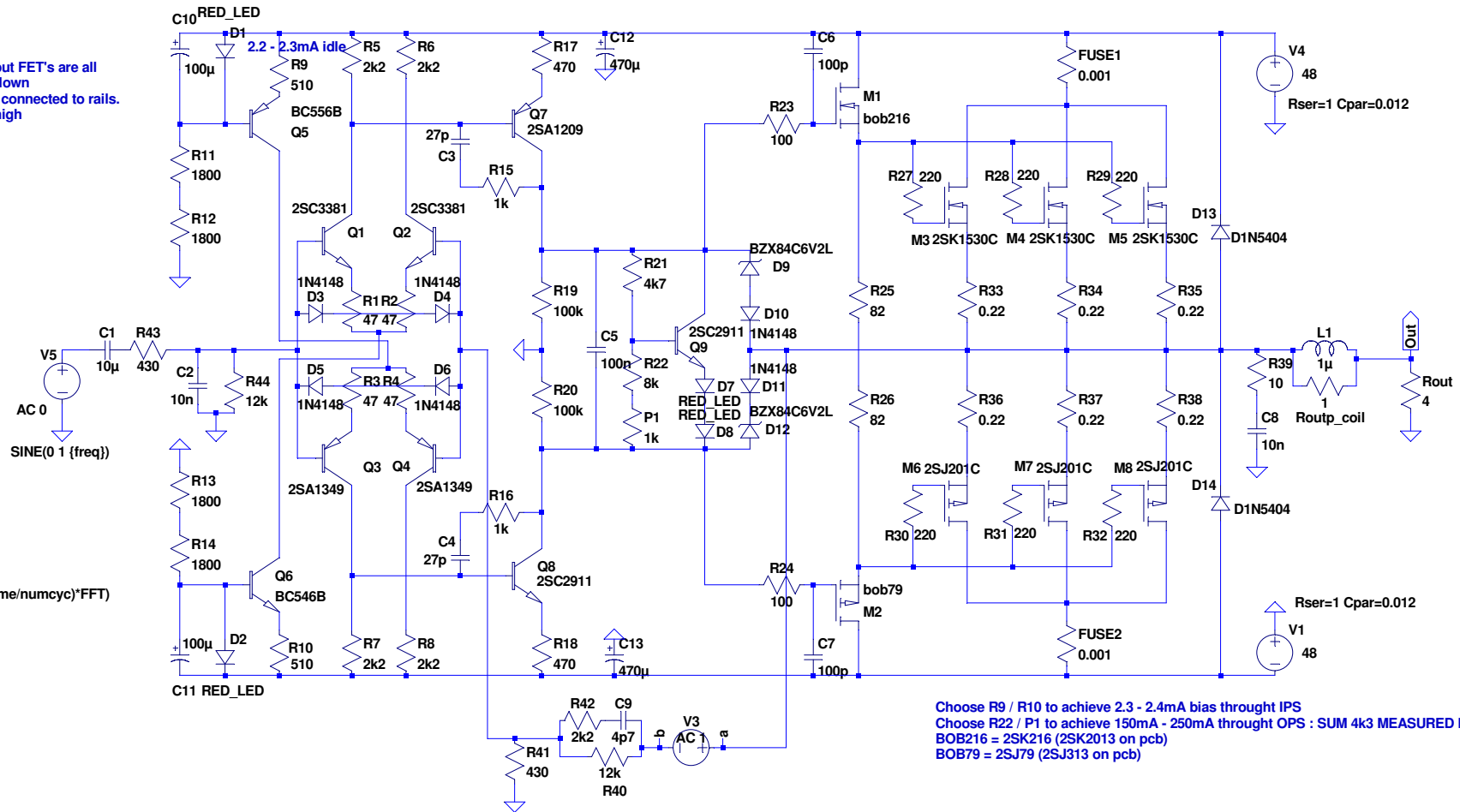
Only output stage has fuses:

- Without zener and 1N4148: output FET's are all dead when one or both fuses blown
- Drivers survive while they keep connected to rails.
- VGS of output FET's will be to high

```

.param Vin=0/15
.options plotwinsize=0
.options numdgt=7
.param Freq=1000Hz
.param numcyc=25
.param dlycyc=5
.param FFT=65536
.param simtime=(dlycyc+numcyc)/Freq
.param dlytime=dlycyc/Freq
.param numsampl=simtime/Freq/((simtime/numcyc)*FFT)
.four {Freq} V(out)
.tran 0 {simtime} {dlytime} {numsampl}
.ac dec 30 1 10meg
.noise V(out) V5 dec 100 .1 1000meg

```



Choose R9 / R10 to achieve 2.3 - 2.4mA bias through IPS
 Choose R22 / P1 to achieve 150mA - 250mA through OPS : SUM 4k3 MEASURED FOR 200Ma
 BOB216 = 2SK216 (2SK2013 on pcb)
 BOB79 = 2SJ79 (2SJ313 on pcb)