A practical approach to amplifier output stage design

There are many requirements for a successful amplifier design. One of the least understood is how to design the output and driver stages to remain within their safe operating areas. Faulty design here can be more than just expensive; the smoking remains are down right embarrassing.

By DAVID EATHER

Many cope with this task by copying from other designs. This is a limiting approach and almost invariably leads to designs with a certain sameness about them. Also, bad design is perpetuated. There is a better way.

This article shows a practical approach to amplifier output stage design and covers the calculation of power supply voltages, output load lines, derating transistor SOAR curves and heatsink selection.

You get nothing for nothing so before you start there is a fair swag of calculations to be done. You also need access to a power transistor data book. The payoff is reliable amplifiers with output power levels customised for your needs.

There are no definitive answers as to exactly how many or what type of transistors you have to use in your design; a lot depends on taste. At the same time, there are certain design rules that should not be transgressed. My method is a simplified approach - the overall aim has been to achieve a reliable design without too much pain. What has been shaved off one area is generally compensated for elsewhere.

For illustration, I will be designing the output and driver stage of a general purpose amplifier capable of 25 watts into 8Ω. The circuit is a simple 10-transistor design as shown in Fig.1.

After a general discussion on each step, I will provide some specific results, so you can check your understanding of the principles being discussed.

Assuming you already know how much power output you want, the first step begins with calculations to find the peak voltage and peak current delivered to the load. Use the following formulas.

$V_{max\ load} = \sqrt{(2 \times P \times Z)}$

$I_{max\ load} = \sqrt{(2 \times P/Z)}$

For my amplifier this works out as:

$V_{max\ load} = \sqrt{(2 \times P \times Z)}$
$= \sqrt{(2 \times 25 \times 8)}$
$= 20$ volts

$I_{max\ load} = \sqrt{(2 \times P/Z)}$
$= \sqrt{(2 \times 25/8)}$
$= 2.5$ amps

Emitter resistors

At this point, I will give a quick mention of the emitter resistors, R1 and R3, on Fig.1. These resistors help provide thermal stability of the output stage bias current and in designs with output transistors in parallel they help to ensure equal current sharing. The higher the resistance the better the thermal stability and current sharing but the more power they waste. The final value is a compromise.

As a guide, you would normally try for about 0.6 volts across the emitter resistors at I_{max} load.

For this design, 0.22Ω should prove adequate. The resistance is a little low but I would not expect any problems for the following two reasons: (1) there is only one output transistor for each rail so there is no current sharing; and (2) I don't intend to set a high quiescent current.

The next step is to work out the required supply voltage ($\pm V_{cc}$). You must consider the requirements of V_{max} load, the voltage drops caused by the driver and biasing circuitry and the voltage drop caused by the emitter resistors in the output transistors, and lastly the ripple voltage (hum and audio signal) on the supply rails ($\pm V_{cc}$).

At this stage, refer to back to Fig.1.

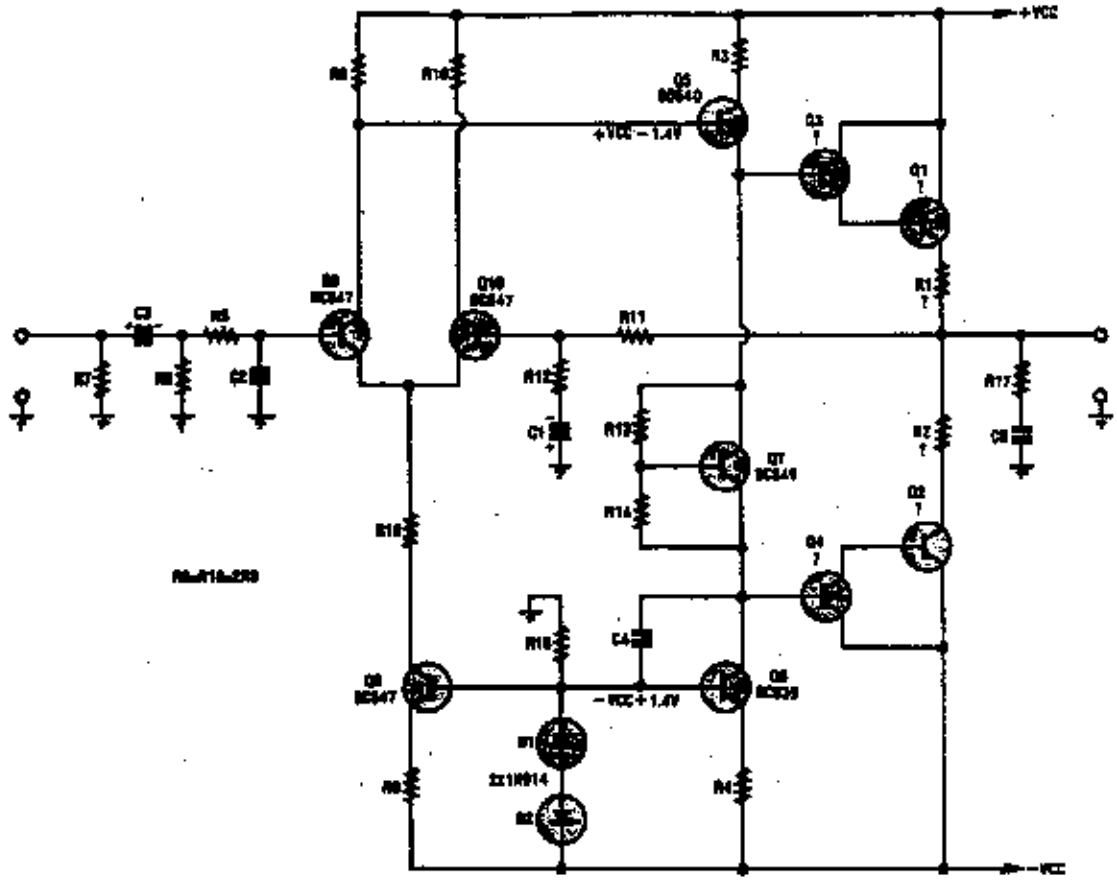

Fig.1: the circuit for a general purpose 10-transistor audio amplifier capable of delivering about 25W into 8Ω. Note that the design uses split supply rails and complementary output stages.

Notice that the bias voltages applied to the bases of Q5 and Q6 are equal. Notice also that the outputs, drivers and pre-drivers are mirror images of each other (R5, Q5, Q2 and Q1 vs R6, Q6, Q4 and Q3). This is a common situation and allows calculation for $\pm V_{cc}$ by considering just the positive side. In cases where the quiescent biasing varies for the positive and negative sides, the $\pm V_{cc}$ rails are worked out separately. Depending on the design, use the larger value for both supply rails.

In this example (see Fig.1 again), there is 1.4 volts across the base-emitter junction of Q5 and R3. We will assume that at full power, the same voltage of 1.4 volts appears between the collector of Q5 and $+V_{cc}$, 0.55 volt peak (I_{max} load x R1) across R1, and 1.6 volts across the base-emitter junctions of Q1 and Q3. This gives a total overhead of 3.55 volts.

Power supply ripple

Next, you have to make an estimate for the ripple on the power supply. For this I like to use what I call Eather's rule of thumb. Stated as a formula it looks like this:

$V_{ripple} = 6300 \times I_{max}\ load/C$

where V_{ripple} is the peak to peak voltage ripple on the power supply and C is the filter capacitor size in microfarads. The capacitors should be a minimum of 100-200µF per watt of output power for a class B amplifier with a full wave rectifier. (Actually, Eather's rule of thumb is not just a whim of mine but is a condensation of the maths for capacitor-input power supplies).

For this example, I have elected to use two 2500µF capacitors for each power supply rail:

$V_{ripple} = 6300 \times I_{max}\ load/C$

$= 6300 \times 2.5/2500$

$= 3.15$ volts

The value for $\pm V_{cc}$ is:

$\pm V_{cc} = V_{max\ load} + V_{ripple}$ + circuit overhead

For my design this becomes:

$\pm V_{cc} = V_{max\ load} + V_{ripple}$ + circuit overhead

$= 20 + 3.15 + 3.55 = 26.7$ volts

This can be safely rounded off to ±27 volts.

Transistor load lines

OK so far? The next step is to figure out the transistor load lines. We are not going to bother with the load lines for resistive loads. These are straight lines and not really the problem for amplifiers. We are concerned with reactive load lines. These show the instantaneous voltage and current flowing through the transistors when driving a complex load impedance such as a speaker.

To do this you need the output power, I_{max} load and $\pm V_{cc}$. You also need the value of the emitter resistors in the output stage (R1, R2 in my case), the power output of the amplifier and the load impedance, Zl.

Before leaping into the computations, we need to make an estimate of the maximum phase shift caused by the inductive portion of the speaker load. 45° seems to be the accepted standard in many electronics magazines and is the value we shall use

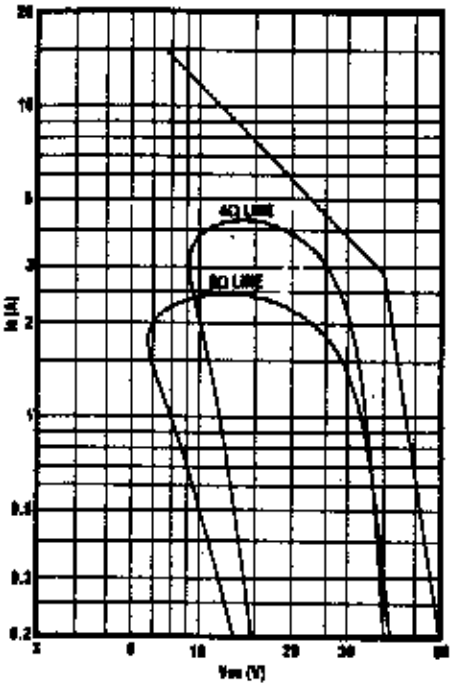

Fig.2: the 4Ω & 8Ω load lines for the output transistors of the amplifier. These curves were plotted using the data shown in Tables 1 & 2 respectively. Note that the load lines should be fully enclosed by the DC SOAR curve of the selected transistor as shown here.

here. However, if you intend to use your amplifier with highly reactive loads such as electrostatic speakers or line transformers, 60° would be a better choice.

Drawing up a table

Now we draw up a table with five columns and 13 rows. The columns are labelled: (ωt - θ), ωt, I_c, V_{ce} and P_{pk}(W). Theta (θ) is the electrical phase shift caused by the speaker. The term "ωt" is the instantaneous phase of the signal frequency and is expressed in degrees. I_c is the instantaneous current through the collector of the output transistor. V_{ce} is the instantaneous voltage across the output transistor. P_{pk}(W) is the instantaneous power dissipated by the output transistor.

The (ωt - θ) column starts at 0 and steps up to 180° in 15° increments. Down the ωt column write the corresponding value of ωt. This is the same as adding the selected value of θ (45° in our case) to the adjacent value of (ωt - θ). This leaves the ωt column with values starting at 45° and ending at 225°.

Start the calculations with I_c, using the formula:

$I_c = I_{max\ load} \times \sin(\omega t - \theta)$

Write down each result in turn for the value of ωt. Next is V_{ce} using the more complex formula:

$V_{ce} = V_{cc} + I_{max\ load} \times Z_l \times \sin(\omega t) + I_c \times R_E$

The column for P_{pk}(W) is calculated by multiplying the collector emitter voltage V_{ce} by the collector current I_c:

$P_{pk}(W) = V_{ce} \times I_c$

Table 1 shows the results for the amplifier under discussion.

Load variations

Now take a deep breath. A general purpose amplifier could drive all sorts of speakers, some with only a very nominal 8Ω impedance. For amplifiers in this situation, it is normal to design the amplifier so that it can safely drive into half the nominal load impedance. This may not be necessary if the amplifier is to drive a known speaker impedance or if using electronic limiting. If electronic limiting is not done carefully though, the amplifier may produce objectionable distortion if pushed hard into a non-resistive load.

The rule of thumb for estimating power output into half the nominal load impedance is that the amplifier will produce about 50% more power. This won't apply if the amplifier has a well regulated power supply and large filter capacitors, in which case the power output will be closer to double. Conversely, if the power supply has poor regulation and small filter capacitors, the amplifier may only deliver a few percent more power into half its nominal load impedance.

First, assume your amplifier will deliver 50% more power. Then you have to check that your amplifier will really deliver this power into the new load. Why? Because if it can, it will have to dissipate a lot more power and we need to know that the transistors can stand this extra stress.

Work out the required value for V_{cc} for the increased power output. This means going through the same procedure you did before, finding the required voltage across the load, the amplifier overhead and the power supply ripple using the new load impedance.

A required value for V_{cc} much larger than that available from your power supply means that the amplifier won't be able to deliver the extra 50% power, except maybe for short peaks. If the required value for V_{cc} is less than the actual supply, the amplifier will deliver a bit more than an extra 50%.

Most times, allowing 50% gives a close estimate of what will actually happen. If, in your case, the value you came up with for V_{cc} was very different, adjust your estimate of output power and go through the checking procedure again.

For my amplifier, half the load impedance equals 4Ω and I expect the amplifier to deliver about 37 watts. The calculations for $V_{max\ load}$ and $I_{max\ load}$ give 17.3 volts and 4.33 amps respectively.

The amplifier overhead goes up by 0.4 volts to 3.95 volts due to the higher current through the emitter resistors. The ripple on the supply also increases to 5.45 volts. So the V_{cc} needed is still about 27 volts.

The next step is to calculate another load line for the new load impedance. Use the new values for Zl and $I_{max\ load}$.

My results for output into a 4Ω load are tabulated in Table 2. We can now draw some conclusions about the possible output transistors. The output devices must have an I_c rated higher than $I_{max\ load}$. The V_{ce} must be twice V_{cc} and the power rating should be at least 50% greater than the largest value for P_{pk}(W) for most designs.

In suggesting 50% more for the power rating of the output transistors, I am assuming power dissipation is the limiting factor and not secondary breakdown. It is just a ballpark figure and may need adjustment.

Output transistors

For your design, you should be able to make an educated guess about what output transistors or combination of transistors you will need to use.

For my job, I will need the output transistors to have an I_c of more than 5 amps, a V_{ce} of 60 volts or more, and a power rating of around 100 watts.

I can now select some possible devices.

For my design, transistor pairs such as the MJE3055/MJE2955, TIP3055/TIP2955, 2N3055/MJ2955 or MJ-15003/MJ15004 could all be suitable.

I won't use the TIP and MJE pairs because the packages are not pin compatible even though they are of-

ten sold as being interchangeable. The mounting tab is on opposite sides when placed into a PC board. This has the potential for mistakes during construction or repairs. Also, the power rating for these transistors is a bit low (only 90 watts). They could work but I will look around for something else.

The 2N3055/MJ2955 pairs have a higher power rating for only a few cents more. This higher power rating could lead to cost and size savings by enabling the use of a smaller heatsink.

The MJ-15003/15004 pairs are nice but relatively expensive. Compared to the 2N3055/MJ2955 pair, they do offer a better current gain-bandwidth product (ft) and would give slightly lower distortion. Also the much higher power rating means I could possibly get away with quite a small heatsink.

Overall, the 2N3055/MJ2955 pairs should perform satisfactorily in my circuit so they are my first choice.

At this stage, the choice of output transistors is no more than an educated guess. It is possible that the transistors may not be suitable. The graph of the load lines, transistor SOAR curves and the heatsink calculations will confirm the final choice.

This is the time to check your transistor data book closely. Enlarge or redraw the safe operating area (SOAR) graphs for the transistors until they are a convenient size. Then plot the

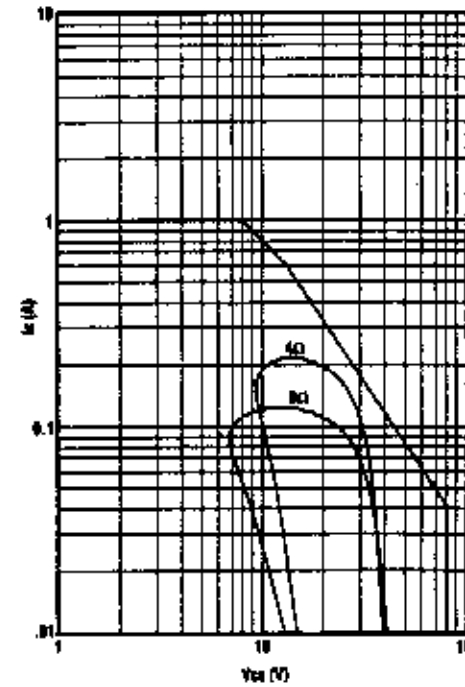

Fig.3: these curves show the load lines for the driver transistors & were plotted using the data shown in Tables 3 & 4. As with the output devices, the load lines must be fully enclosed by the DC SOAR curve of the transistor.

load lines for the amplifier using the points you calculated above.

Fig.2 is my plot for the 4Ω and 8Ω loads using the data in Tables 1 & 2. You may be used to seeing these load lines in text books on graphs with a linear scale and think mine look a bit strange. Don't worry, they are the same type of graph only the scales are logarithmic.

Notice how the 2N3055 SOAR curve fully encloses the load lines. If this were not the case, then the amplifier may die on the first occasion it is required to give a big burst of power.

Make sure the load lines are fully enclosed by the DC SOAR curve of your transistor. The fully enclosed load lines show that the selected power transistor can work in the design.

Driver transistors

Now we come to the driver transistors.

The first step is to calculate the load impedance presented to the driver transistors. In my case, it is simply the speaker impedance multiplied by the minimum beta of the output transistor over the range of currents of interest (0 to I_{max} load).

For the 2N3055, the minimum beta is 20.

Calculate I_{max} for the driver by dividing I_{max} load by the beta of the output transistor. If your circuit calls for it, make sure you add in any other currents the driver transistor must supply.

Now calculate points for the load lines for the driver transistors in the same way as for the output transistors. Remember to do this for half the nominal load impedance if applicable.

My results are tabulated in Tables 3 and 4 while Fig.3 shows the plotted load lines. Note that, as with the output devices, these load lines must be fully enclosed by the DC SOAR curve of the selected transistor.

Go through the same selection procedure as you did for the output transistors.

For my case, a look down the tables on this page shows a peak power dissipation of 4.06 watts and a maximum current of 216mA. Notice that even at these modest power levels, small signal transistors like the BC546/7/8 aren't able to cope. Be wary of designs that suggest they will. I will try a BD139/BD140 pair for the driver transistors.

Next month, we will see if a pair of BD139/BD140 transistors is up to the task of being driver transistors in the circuit of Fig.1. I think that they will but we'll find out for sure, next month. See you then. SC

Table 1

ωt-θ	ωt	Vce	Ic	Ppk(W)
0	45	12.858	0.000	0.000
15	60	9.537	0.647	6.171
30	75	7.406	1.250	9.258
45	90	6.611	1.768	11.687
60	105	7.205	2.165	15.600
75	120	9.148	2.415	22.091
90	135	12.308	2.500	30.770
105	150	16.469	2.415	39.769
120	165	21.347	2.165	46.218
135	180	26.611	1.768	47.042
150	195	31.901	1.250	39.877
165	210	36.858	0.647	23.848
180	225	41.142	0.000	0.000

Table 2

ωt-θ	ωt	Vce	Ic	Ppk(W)
0	45	14.753	0.000	0.000
15	60	11.754	1.121	13.172
30	75	9.794	2.165	21.204
45	90	9.006	3.062	27.576
60	105	9.445	3.750	35.418
75	120	11.080	4.182	46.343
90	135	13.800	4.330	59.755
105	150	17.420	4.182	72.858
120	165	21.692	3.750	81.344
135	180	26.326	3.062	80.605
150	195	31.007	2.165	67.129
165	210	35.414	1.121 3	9.687
180	225	39.247	0.000	0.000

Table 3

ωt-θ	ωt	Vce	Ic	Ppk(W)
0	45	12.858	0.000	0.000
15	60	9.537	0.032	0.309
30	75	7.406	0.063	0.463
45	90	6.611	0.088	0.584
60	105	7.205	0.108	0.780
75	120	9.148	0.121	1.105
90	135	12.308	0.125	1.538
105	150	16.469	0.121	1.988
120	165	21.347	0.108	2.311
135	180	26.611	0.088	2.352
150	195	31.901	0.062	1.994
165	210	36.858	0.032	1.192
180	225	41.142	0.000	0.000

Table 4

ωt-θ	ωt	Vce	Ic	Ppk(W)
0	45	14.781	0.000	0.000
15	60	11.789	0.056	0.659
30	75	9.834	0.108	1.062
45	90	9.048	0.153	1.382
60	105	9.486	0.187	1.774
75	120	11.117	0.209	2.319
90	135	13.831	0.216	2.987
105	150	17.442	0.209	3.639
120	165	21.705	0.187	4.060
135	180	26.328	0.153	4.021
150	195	30.997	0.108	3.348
165	210	35.394	0.056	1.979
180	225	39.219	0.000	0.000