# A Low-Voltage MOSFET with Small on-Resistance: an Extended Characterization in High-Efficiency Power Converter Applications

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**Abstract - The paper deals with a new concept applied in designing low-voltage power MOSFETs, which are suitable for high-current low-voltage converter applications. The layout of the proposed device family overcomes the traditional cell structure by a new strip-based geometry. They present interesting characteristics due to the advanced design rules typical of VLSI processes and strong reduction of the on-state resistance. Further, the technology process allows a significant simplification of the silicon fabrication steps, thus allowing enhancing the device ruggedness. The high current handling in switching conditions (up to 150 A) with a breakdown voltage in the range between 20-50 V in a convenient package solutions allow to give the correct answers to the low-voltage range switch applications. The paper starts with the description of the main technology issues in comparison with that of standard devices, particularly focusing on the innovations and the improved performances. Moreover a detailed characterization of the MOSFET behavior in traditional test circuit as well as in an actual AC motor drive for wheel chair applications is presented and discussed.**

## I. INTRODUCTION

Higher efficiencies are expected nowadays in the field of power converters for battery powered systems. As industrial and commercial applications of these systems are more and more increasing (laptops, portable equipment, home appliances, electric assisted bikes, electric scooters, wheel chairs, mobiles, etc.), higher efficiencies become of major interest in order to meet the user requirements of long-lasting behavior with the same battery charge. To do that, researchers have done dramatic efforts in designing new converter structures, in increasing the converter switching frequency and in conceiving innovative power devices.

Battery powered systems require, generally speaking, low-voltage switching devices (<100 V), and power MOSFET devices dominate in this voltage range due to their attractive characteristics of high switching speed and easy driving capability. On-state losses of MOSFETs are of major concern on their total power loss balance, especially in case of converters with low or medium switching frequency. Since on-state losses depend on the drain-source resistance ($R_{on}$), which is strictly related to the structure design, many modern MOSFETs are realized with a cell based layout which determines low on-state resistance. The increase of the cell density allows to further reducing the on-state resistance, thus increasing the current capability per device area-unit. However, for today state-of-the-art MOSFETs ulterior reduction of the on-state resistance by this conventional layout is impeded since this approach is reaching its own physical limit [1]. The need of innovative approaches arises in order to overcome the limit of this technology.

The strip-based layout is a new approach [2], which allows using a simplified process for implanting the body and isolating the poly silicon gate from the source. The new technology is very effective in eliminating the limit of the cell-based layout, which relies on the capability to open smaller and smaller windows on the poly silicon area in order to obtain greater cell-density figures. With the strip-based layout, MOSFET devices show improved performances and a simpler manufacturing process. Moreover they benefit of the well-established and advanced design rules typical of VLSI processes. On-state resistance values as low as 1.2 mΩ can be reached, but the overall MOSFET design must account for the best trade-off of a merit figure which is the product of the on-state resistance and the gate charge values ($R_{on}Q_G$).

In this paper the main issues of the new technology are briefly recalled, and the device structure is described and discussed. The static and dynamic characteristics of devices belonging to this new family of MOSFETs are presented and compared with those of more traditional ones. Conventional experimental tests have been carried out and are discussed aiming to determine the impact of turn on and turn off energy loss [3]. A low-voltage battery-powered converter for wheel chairs is used as a workbench for an application-oriented characterization. The drive has been designed and now is in the final stage of development as a laboratory prototype. Some relevant tests are reported and discussed. A detailed analysis is done on the conduction and switching losses and the thermal behavior in the actual application.

0-7803-7114-3/01/$10.00 (C) 2001

## II. Main Technology Issues of Strip-Based MOSFET

The structure of a strip-based MOSFET device overcomes the limit of a cell structure. In Fig. 1 the geometry of the two differently conceived devices are shown. The main differences between a standard square-cell layout and the strip implementation may be better understood by inspecting Fig. 2. In the conventional cell structure shown, all subsequent contacts and isolation openings must be confined and aligned inside the largest square windows opened on the poly silicon layer whose side is $L$ in Fig. 2. That dimension depends on the alignment, the resolution, and the process tolerances and can be expressed as:

$$L=c+2b+2t \quad (1)$$

where:

- $c$ is the contact dimension for the body region imposed by the resolution of the photolithography equipment;
- $b$ is the contact dimension for the source region which depends on the alignment capability and on the metallization process;
- $t$ is the separation (isolation) between the poly and source metal and is controlled by the alignment feature.

Consequently, the standard cell layout depends on three feature sizes.

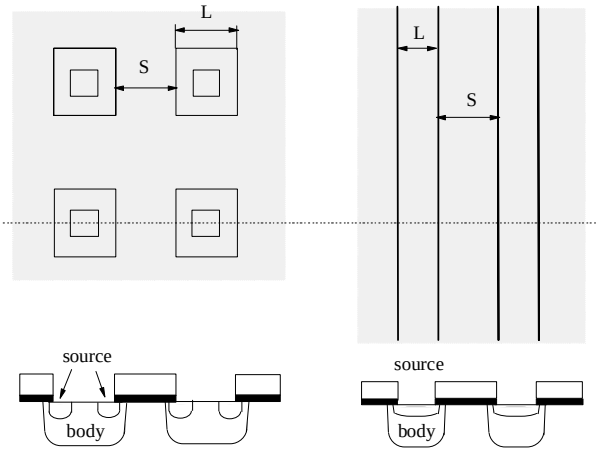


Fig. 1. Cell-based and strip-based structures of two power MOSFETs.

In the strip-based layout process an intermediate dielectric layer is obtained after growing the gate oxide and depositing the poly silicon. In such a sandwich structure parallel strips are opened through an appropriate photo masking process. After implanting the body, the source regions are created by using a sort of small rectangle (patches) masking. The longer sides of the patches are perpendicular to the strips in such a way that they do not need to be aligned within the strip but only along their spacing, which normally is larger than the opening, thus avoiding any alignment problem. The next step is to isolate the poly silicon along the stripe's periphery thanks to the spacer process. This is achieved by etching the dielectric material originally deposited and creating "hills" on the sides of the strips. Finally, Aluminum deposition is done in order to contact the strips, and the fabrication flow chart is completed.

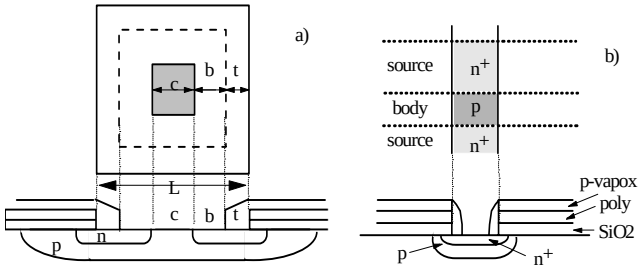


Fig. 2. Cell-based and strip-based structures of two power MOSFETs showing the key parameters of the elemental component of the geometry.

The source mask does not need to be aligned within the strip itself, the only critical parameter is the width of the strip (see Fig. 1), which depends on the equipment resolution. As can be argued from the above description, the process benefit of a reduced number of feature sizes since now it is dependent only on a single feature size, and higher packing densities can be obtained in comparison to the conventional cell-geometry process. The new process is also named extremely high density (EHD) referring to the possibility of getting devices with very high equivalent cell densities.

## III. Static and Dynamic Behavior of the New Device

The resulting MOSFET device of the strip-based process shows very interesting characteristics: extremely high packing density and low on-state resistance, rugged avalanche characteristics, and less critical alignment steps. First of all we have selected the device (STB80NF55 type) which was the candidate for the actual application in an AC drive. The drive is described with more details in the next section. The main electrical quantities of the component are: rated current $I_D$=80 A @ 25°C, breakdown voltage $BV_{DSS}$=55 V, on-state resistance $R_{on}$<0.0065 Ω. The device is encapsulated in a TO-263 ($D^2PAK$) package. The gate charge trace is shown in Fig. 3; at a supply voltage $V_{DD}$=44V, and $I_D$=80 A, and $V_{GS}$=10 V the charge is $Q_G$=180 nC.

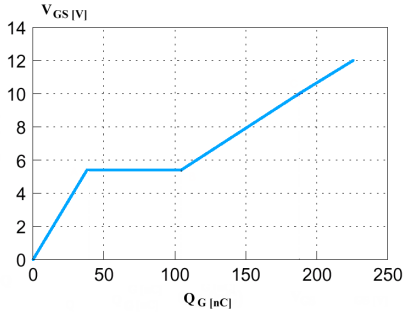


Fig. 3. Gate charge curve of the MOSFET under test (STB80NF55L) at $V_{DS}$=44 V and $I_D$=80 A.

A preliminary characterization in a dc chopper working on inductive load has been done. The trace of a turn-off switching behavior on inductive load at 80 A with a dc bus of 34V and $R_G$=10 Ω, at room temperature, is reported in Fig. 4. The turn-off energy loss measured in this test are $E_{off}$=470 µJ. Looking for the specific application supplied at a dc bus of 24 V, several commutation tests (turn on and turn off ) have been done at this voltage while the current assumed a variable value. The energy losses in such conditions are reported in Fig. 5. Linear dependence of the energy versus the switched current is evident both for the turn on and turn off transients.

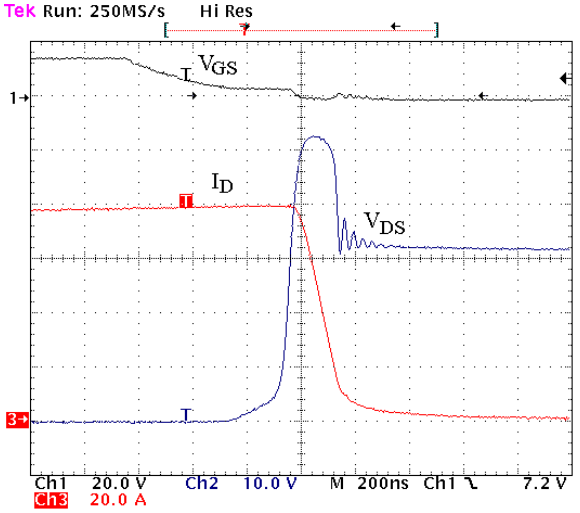


Fig. 4. Turn-off transient on inductive load at 80A and supply voltage 34V $V_{DS}$=10 V/div, $I_D$=20 A/div, $V_{GS}$=20 V/div, $t$=200 ns/div.

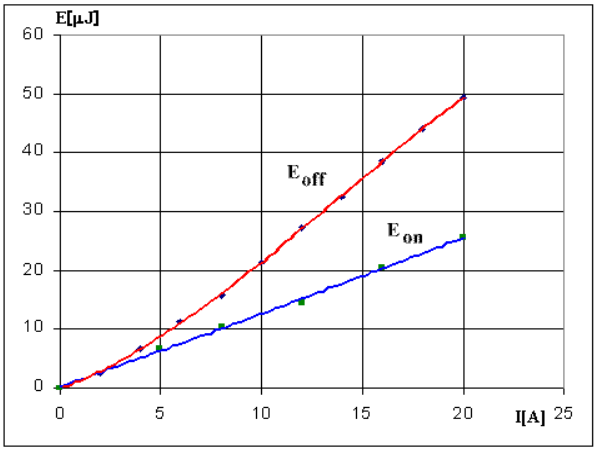


Fig. 5. Energy losses during turn off and turn on transients versus the drain current at $V_{DS}$=24 V.

Since in bridge topology the performances of the body-drain diode could be conveniently exploited, the characteristics of this intrinsic diode have been tested. The main data, at rated current conditions, are reported in Table I. A favorable characteristics of this internal body-drain diode is its high d$v$/d$t$ capability, so crucial in all bridge topologies such as motor drives or uninterruptible power supply (UPS). For the used device the allowed limits is 10 V/ns. Finally in Fig. 6 are reported the static characteristics of the new MOSFET. In forward conduction (positive drain voltage) is traced the $I$/$V$ characteristic of the MOSFET. In reverse conduction two static characteristics are reported relative to the MOSFET and the intrinsic diode: at zero source-gate voltage the current will flows exclusively as a diode current; with a gate bias voltage the current will flow through the MOSFET as in the case of synchronous rectifier applications.

TABLE I
MAIN CHARACTERISTICS OF THE BODY-DRAIN DIODE AT RATED CURRENT
CONDITION: $V_{DS}$=24V, $I_D$=80A d$i$/d$t$=100 A/µs.

| | $T$j=25°C | $T$j=150°C |
|---|---|---|
| $I_{rm}$ [A] | 5.8 | 6.5 |
| $t_{rr}$ [ns] | 80 | 90 |
| $Q_{rr}$ [nC] | 230 | 295 |

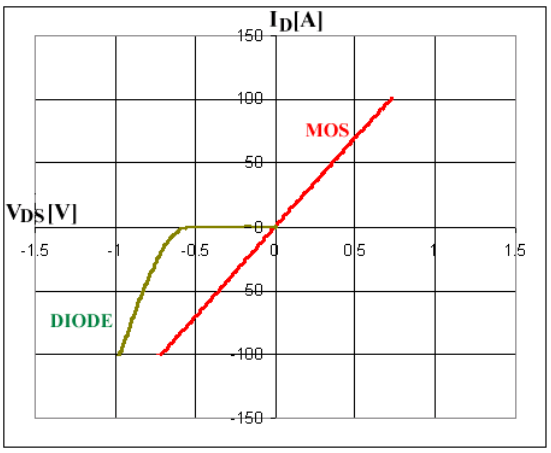


Fig. 6. Static characteristics of the new MOSFET and its body-drain diode at a temperature of 125 °C.

## IV. THE LOW VOLTAGE AC MOTOR DRIVE APPLICATION

The new device has been tested in a low voltage ac drive for wheel chairs, which is in an advanced stage of realization as laboratory prototype. Two lead-acid batteries, in series connection with a rated voltage of 24 V and 45 Ah rated capacity, power the traction system. In the past such low voltage applications required the paralleled operations of many MOSFETs, since the on-state resistance of a single device was unacceptably high. In our case a rated current of 80 A will produce in the used MOSFET about 0.5-0.7 V which is quite acceptable.

The actuators of the electrical drives are two permanent magnet brushless motors [3], rated speed 110 rpm, rated torque 20 Nm, rated power 250 W, rated current 15 A, number of rotor poles 16, equipped with a coaxial position transducer (absolute encoder). A three-phase current

regulated pulse width modulated (CRPWM) inverter feeds each motor. In some critical conditions of load (tentative of the user to overcome a step) the motor should be able to develop five times the rated torque, and consequently the current fed by the inverter should increase up to 70-80 A for several tenth of seconds. The inverter is controlled by a tolerance (or hysteresis) band technique [4], which allows supplying sinusoidal-shaped currents which values change according to the requirements of the load. A simplified schematic of the drive system is shown in Fig. 7.

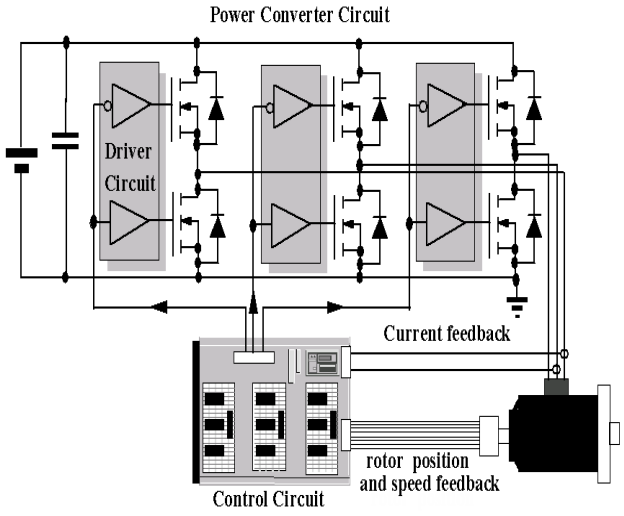


Fig. 7. Schematic of the ac drive used as a benchmark to derive the characterization of the new device in an actual application.

The devices in the full bridge inverter receive the command at a switching frequency $f_S$, which is mainly depending on the width of the hysteresis band. An acceptable value of such a band is 2-4%, and determines in the case study with a figure of 4% a (quasi constant) commutation frequency of 24.5 kHz. Fig. 8 shows a detail of the phase current and the switch control voltage. Fig. 9 shows the experimental traces of the three sinusoidal currents feeding the motor. The fundamental inverter frequency is 0.5 Hz according to the need of the low speed on the wheel shaft.

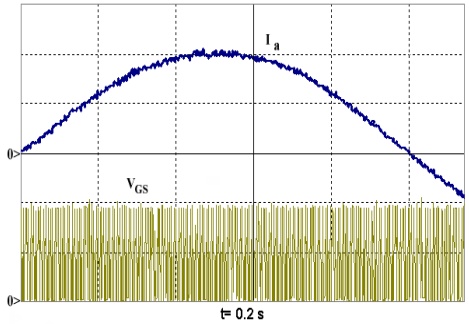


Fig. 8. Traces of a phase current (frequency 0.5 Hz) and the switch control voltage while the motor drive is working at full load. $I_a$=10 A/div, $V_{GS}$=10 V/div, $t$=200 ms/div.

The spectra of the voltage and current traces in Fig. 8 are shown in Fig. 10. In the case analyzed the fundamental component of current is at about $f_1$=11,5 Hz, which is the frequency carrying the active power used for the traction needs, while the harmonics generated by the PWM switching are located at $f_S$=24 kHz and its multiple.

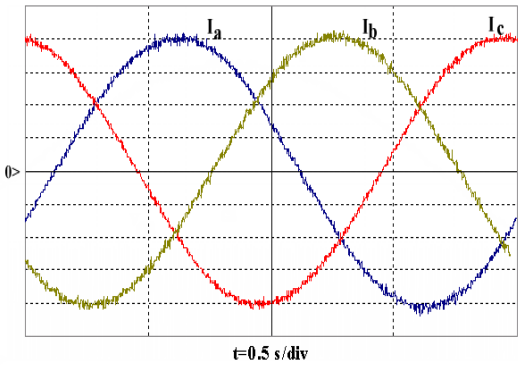


Fig. 9. Traces of the motor phase currents while the drive is operating at a fundamental frequency of 0.5 Hz. $I_{a,b,c}$=5 A/div, $t$=500 ms/div.

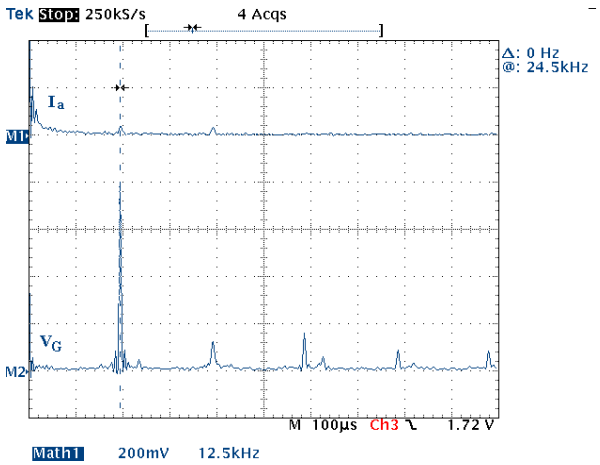


Fig. 10. Harmonic spectra of the current and voltage traces which are shown in Fig. 8.

### *A. Power Losses Estimation*

The device power losses are related to the switching behavior, and the on-state condition. In a generic $j$-th switching cycle the energy losses at turn-on, turn-off, and on-state condition are expressed respectively by:

$$E_{on,j} = \int_0^{t_{on,j}} v_{DS,j} i_{D,j} dt \quad (2)$$

$$E_{off,j} = \int_0^{t_{off,j}} v_{DS,j} i_{D,j} dt \quad (3)$$

$$E_{con,j} = \int_0^{t_{con,j}} v_{DS,j} i_{D,j} dt = \int_0^{t_{con,j}} R_{on} i_{D,j}^2 dt \quad (4)$$

At a constant switching frequency $f_S$, the turn on, turn off and conduction power losses in a device of an inverter leg

(upper or lover device), working with sinusoidal shaped waveform of the current, are expressed respectively by:

$$P_{on} = \frac{1}{2}\sum_{1}^{f_s}{}_j \int_0^{t_{on,j}} v_{DS,j} i_{D,j} dt \quad (5)$$

$$P_{off} = \frac{1}{2}\sum_{1}^{f_s}{}_j \int_0^{t_{off,j}} v_{DS,j} i_{D,j} dt \quad (6)$$

$$P_{con} = \sum_{1}^{f_s}{}_j \int_0^{t_{con,j}} R_{on} i_{D,j}^2 dt \quad (7)$$

where $j$ is the variable accounting for the number of switching cycles per second, which in turn means by definition the switching frequency $f_s$. With reference to the used PWM technique, the current through the devices is sinusoidal-shaped, while the voltage across the device is the dc rail voltage maintained at constant amplitude.

The use of relations (5-7), which is very simple in case of a chopper circuit operated at constant load current [3-6], is more complicated in this case. This is due to two main reasons: the non-linearity of both the instantaneous voltage $v_{DS}$ and the instantaneous current $i_D$ during the switching transient, and the sinusoidal variation of the load current. From inspection of the data reported in Fig. 5 we can observe the nonlinear trend of the switching losses as function of the amplitude of the drain current at a constant clamp voltage. Thus, obtaining any closed equation from relations (5-6) is practically prevented.

Eq. (7) can be evaluated straightforward by a simple formula according to the following consideration. Due to the use of the body-drain diodes as antiparallel devices, while for example an upper device of the inverter leg is in turn off condition a positive current will flow through the body diode of the lower device [7-8]. This happens surely during the dead time of the inverter, but the current can switch in the channel of the lower MOSFET once that its gate is positive biased. A same behavior applies for the lower device in blocking state and the upper device conducting firstly through the diode and then through the channel. Hence, that means from an effective point of view that the conduction losses of a switch during a fundamental period $T_1$ of the carrier are due to half sinusoidal waveform of the current. In fact, the current flows through the MOSFET (forward conduction, positive current) or through the intrinsic diode (dead time, and reverse current), or through the MOSFET in reverse conduction and gate biased. The behavior of the MOSFET while is in such a reverse conduction, via the intrinsic body diode or via the channel, is clearly shown in Fig. 11, where is also evident the time interval adopted as dead time of the inverter.

Accordingly, the conduction power loss can be calculated by:

$$P_{con} = \sum_{1}^{f_s}{}_j \int_0^{t_{con,j}} R_{on} i_{D,j}^2 dt \cong R_{on} \frac{1}{T_1} \int_0^{T_1/2} \left( \sqrt{2} I_{rms} \sin \frac{2\pi}{T_1} t \right)^2 dt =$$

$$P_{con} = 0.5 R_{on} I_{rms}^2 \quad (8)$$

Finally the total power losses can be evaluated by:

$$P_{tot} = P_{on} + P_{off} + 0.5 R_{on} I_{rms}^2 \quad (9)$$

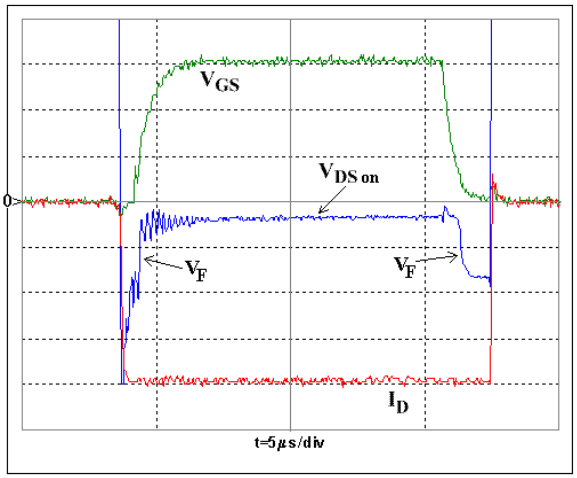


Fig. 11. Reverse conduction of the power MOSFET through the intrinsic body diode or through the channel.
$I_D$=5 A/div, $V_F$=0.5 V/div, $V_{GS}$=5 V/div, $t$=5 µs/div.

### *B. Power Losses Measurement from the Thermal Behavior*

The total power losses $P_{tot}$, in the steady-state conditions as before described, are related to the actual heat sink temperature by relation:

$$P_{tot} = \frac{T_H - T_A}{R_{th,HA}} \quad (10)$$

where $T_H$ is the heat sink temperature, $T_A$ is the ambient temperature (25 °C), and $R_{th,HA}$ is the thermal resistance between the heat sink and the ambient. Relation (10) can be used to indirectly measure the total power losses, by measuring the ambient and heat sink temperatures and knowing the thermal resistance.

First of all the thermal resistance has been experimental established, by means of specific test with known power condition, at $R_{th,HA}$=15 °C/W accounting for the actual layout. Hence, the total power losses expressed by the relation (9) have been evaluated by (10) measuring the temperatures in the prototype in several loaded conditions. A separation in switching and conduction power losses has been carried out by calculating $P_{con}$ through equation (8) and $P_{sw}$ as difference of the total and the conduction power losses. The main results obtained are reported in the Table II.

The same test procedure has been repeated with a different hysteresis band (about 18%), which implies a

different ripple on the phase currents of the motor, in order to determine the influence of the switching frequency on the thermal behavior of the devices. In such a condition the switching frequency reduced to 1 kHz. The traces of the motor currents for this new operating condition are reported in Fig. 12. The ripple is increased but is yet tolerable. In Fig. 13 are given the whole results of the two test conditions with different switching frequencies; the traces are relative to the total power losses and the conduction ones.

TABLE II
THERMAL BEHAVIOR OF THE POWER MOSFET AT DIFFERENT CURRENT CONDITIONS: HYSTERESIS BAND 4%.

| $I$ [A] | $T_H$ [C] | $P_{tot}$ [W] | $P_{con}$ [W] | $P_{sw}$ [W] | $R_{DSon}$ [mΩ] |
|---|---|---|---|---|---|
| 5.74 | 50.2 | 1.68 | 0.06 | 1.62 | 6.90 |
| 9.08 | 60.8 | 2.39 | 0.15 | 2.24 | 7.22 |
| 10.30 | 64.3 | 2.62 | 0.19 | 2.43 | 7.32 |
| 13.13 | 71.3 | 3.08 | 0.32 | 2.76 | 7.53 |
| 15.00 | 76.0 | 3.40 | 0.43 | 2.97 | 7.68 |
| 19.70 | 95.0 | 4.67 | 0.80 | 3.87 | 8.25 |

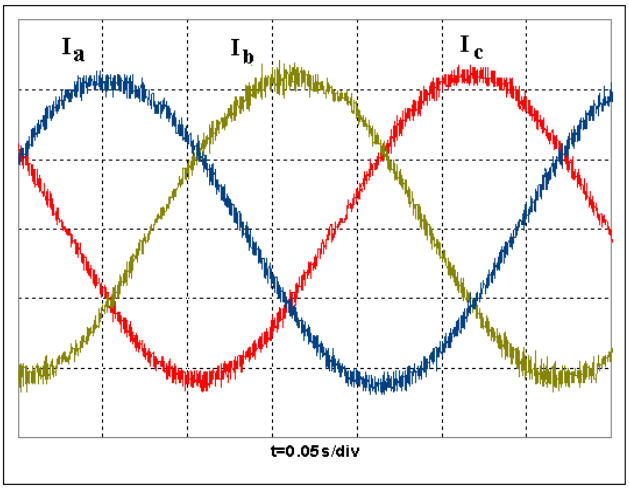


Fig. 12. Experimental traces of the phase currents. The switching frequency of the inverter is 1 kHz as consequence of the increased tolerance band of the hysteresis comparators. $I_a$=10 A/div, $t$=50 ms/div.

## V. CONCLUSIONS

A full characterization of the device has been presented. First of all the MOSFET has been tested in order to evaluate the static and dynamic performances by traditional procedures. Then the device behavior has been investigated in a conventional chopper circuit, and several switching cycles have been performed in order to define, at constant clamp voltage, the trend of the energy losses as function of the drain current. A full characterization on a specific battery-powered converter has been presented and discussed. In particular, an analysis of the power losses has been previously carried out aiming to calculate and separate the switching and conduction contributions in such an application. Finally an experimental validation by a steady state thermal behavior has been performed to apply the analytical relations that have been determined. The results are interesting thus encouraging the use of the internal diode as antiparallel diode. In conclusion, the power MOSFETs presented has been demonstrated to be very suitable for inverter bridges in the field of commercial and industrial applications working at low voltage.

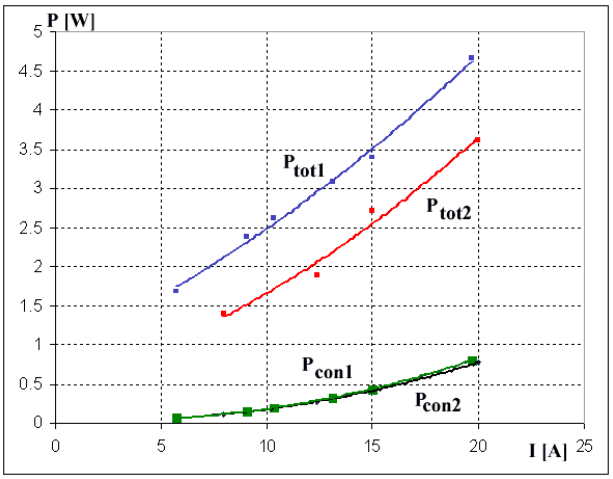


Fig. 13. Total power losses at two switching frequencies (1 kHz and 24,5 kHz), and conduction losses in a power MOSFET of the inverter leg.

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