utterance where the degree of slurring and reduction is high.) When speech recognition is viewed from the level of the phonetic segment or that of the phonetic feature the problem of finding *invariant* acoustic correlates of such categories comes to the foreground. This problem has been subject to a great deal of attention during the past few decades. It will no doubt stay with us even if we manage to construct models that capitalize on grammatical and semantic redundancy. However, it is likely to reduce considerably in magnitude as progress is made in widening the research perspective on human speech perception.

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An Audio Power Amplifier for Ultimate Quality Requirements

JAN LOHSTROH and MATTI OTALA

Abstract—A 50 W/4 Ω complementary symmetry audio amplifier concept is described. The amplifier is designed to meet ultimate quality requirements with particular emphasis on lack of transient intermodulation distortion. Excellent phase and amplitude linearity is obtained using low feedback value, class A operation for most of the signal time, and a fully symmetric dc-coupled high frequency design.

Introduction

It is better to overestimate than to underestimate the capability of the ear to detect amplifier imperfections. Recently a number of theories and experiments concerning phase linearity requirements, transient intermodulation effects, and psychoacoustics [1]-[3], [7]-[11] have shown that some of the basic "truths" of audio amplifier design should be revised.

The purpose of this work is to try to meet the new, drastically different requirements. The approach chosen is to avoid all apparently "elegant" tricks frequently employed (bootstrapping, positive feedback, distortion compensation, higher feedback for dc than ac, gliding bias, etc.) and to produce a state-of-the-art amplifier for ultimate quality requirements.

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Transient Intermodulation Distortion

This type of distortion occurring at nonstationary signals, is caused by the feedback [1], [2] and seems to plague many commercial amplifiers [2]. When an input signal, having a sufficient amplitude and a higher frequency than the power amplifier *open-loop* cutoff frequency, is presented in the input, overshoots in the internal loop drive voltage of the feedbacked amplifier are produced. Depending on the value of feedback, these overshoots may be several hundred times greater than the nominal value of this voltage. Consequently, they will be clipped in the driver stages of the amplifier if sufficient overload margins do not exist, and will then produce momentary 100 percent intermodulation bursts. Because audio signals usually have their maximum slopes around the zero signal level, these distortion bursts usually occur in this region. The audible effect therefore resembles high-frequency crossover distortion and according to recent studies [3], the ear seems to be extremely sensitive to it. If weak, this distortion is not perceived as usual distortions, but creates a sort of "metallic, annoying" sound.

To avoid transient intermodulation distortion, the *open-loop* frequency response of the power amplifier should exceed the preamplifier frequency response. This open-loop response is generally governed by the lag compensation network of the amplifier. The amount of lag compensation necessary to stabilize a given amplifier, in turn, is directly proportional to the amount of feedback used. The designer therefore has a difficult tradeoff dilemma: in order to decrease the usual steady-state harmonic and intermodulation distortions, he would like to use as much feedback as possible. This would, however, drastically decrease the open-loop frequency response owing to the necessary heavy compensation, and thus increase transient intermodulation distortion.

The optimum feedback has a value where all these distortion phenomena contribute equally to the audible distortion sensation. The recent tendency to use much higher values of feedback than necessary has radically upset this balance.

The various means of minimizing the transient intermodulation distortion include [4]:

1) good high-frequency design along with the use of lead compensation instead of lag compensation within the feedback loop, and

2) use of low value of feedback.

The first of these methods requires gain reserves from the amplifier stages in order to make effective lead compensation possible, and the second requires very good open-loop linearity, because heavy feedback is not present to decrease static harmonic and intermodulation distortions. If the open-loop frequency response of the amplifier is higher than the audible frequency range, even moderate feedback may yield a power amplifier small-signal frequency response of the order of 1 MHz, and the limiting of the frequency response to 20 kHz [6] must be accomplished with a passive filter in the preamplifier.

Phase and Amplitude Linearity

Recent psychoacoustic experiments have convincingly shown that the ear is sensitive to phase relationships of the components of an audio signal [7]–[10]. It seems that only 10° deviation from exact phase linearity can be tolerated in the audible frequency range for the most critical requirements in direct field listening conditions. If phase correction networks are not used, this implies an amplifier closed-loop small-signal frequency response in excess of 200 kHz.

The important frequency response parameter is the power bandwidth, which requires redefinition. At present it is measured at the distortion level of 1 percent (European DIN 45 500 requirement) or even at the amplifier limiting level. Especially at the critical high frequencies, severe distortion is usually present far below the limiting level, and the occurrence of two or more high-frequency signals will cause strong difference intermodulation products to fall within the audible frequency range.

The power bandwidth should therefore always be measured at a specified distortion level. For professional quality amplifiers we propose the use of 0.2 percent total harmonic distortion as a measurement standard.

This measurement is fairly straightforward and simple, the only precaution being the disconnection of possible output filter elements (i.e., L_1-R_{35} and C_7-R_{34} in Fig. 1), which may attenuate the higher harmonics.

The definition of power bandwidth should then be the -3 dB points of the measured response, i.e., the half-power points. It should exceed the preamplifier frequency range in order to prevent distortion and amplifier overload due to high frequency components of the signal.

Other Design Criteria

The ear seems to be very sensitive to amplifier imperfections around the zero output level. Daugherty and Greiner [11] originally proposed that amplifiers should operate in class A for most of the signal time, and derived the corresponding A- to B-class transition level to be about 17 dB below the full output power. This almost-class-A-operation completely eliminates crossover distortion and greatly diminishes class B-type asymmetries, which are easily caused by improper design, or even in well-designed fully complementary symmetry amplifiers by fundamental differences in the p-n-p and n-p-n power transistors.

It is common practice to employ higher feedback values for dc than for ac, motivated by the apparent increase of dc stability. However, this argument is not valid, because a sufficient dc stability can easily be achieved without this kind of trick by proper use of circuit symmetry and temperature compensation. On the other hand, a high dc feedback value can cause exotic clipping and distortion effects, and infrafrequency rumble, because of open-loop B-class gain asymmetries that force dc level adjustment transient through the feedback loop every time the signal amplitude changes. These effects often remain undetected in usual amplifier measurements, as they usually manifest themselves only in tone burst tests and noise cross-correlation tests, and are not discernible with steady-state sinusoidal signals.

It is therefore desirable to make the feedback value the same for ac and dc, at the same time eliminating a number of undesirable large capacitors, which always seem to be sources of trouble in class AB amplifiers.

The use of usual driver collector bootstrapping can give rise to asymmetries and poor clipping behavior. These problems can be eliminated by the use of symmetrical drivers that, apart from good linearity and ideal limiting characteristics, also lend themselves to integration of the power amplifier pre-stages.

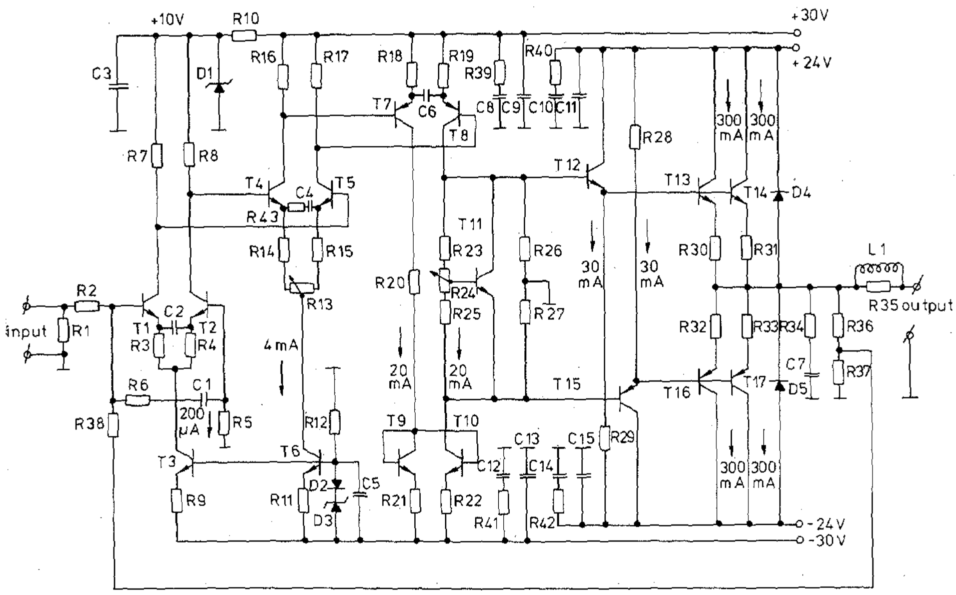


Fig. 1. Circuit diagram of the amplifier. In order to make the diagram clearer the short-circuit and overload protection circuitry is not shown. The components are as follows:

$T1$ and $T2$	= dual transistor pair BCY 87	$R1$, 2, 10	= 6.8 k	$R23$	= 1.5 k
		$R3$, 4 metal film	= 1 k	$R24$ (pot.)	= 1 k
$T4$ and $T5$	= dual transistor pair BCY 89			$R25$	= 470 Ω
		$R5$	= 10 k	$R26$, 27, 36	= 2.2 k
$T3$, 6	= BC 107	$R6$	= 470 Ω	$R28$, 29	= 820 Ω/ 1W
$T7$, 8, 15	= BD 140	$R7$, 8	= 22 k	$R30$, 31, 32, 33	= 1 Ω/2 W
$T9$, 10, 11, 12	= BD 139	$R9$	= 68 k	$R34$	= 12 Ω/2 W
$T13$, 14	= BD 203	$R11$	= 3.3 k	$R35$	= 2.2 Ω/2 W
$T16$, 17	= BD 204	$R12$	= 4.7 k	$R37$	= 390 Ω
$C1$	= 220 pF	$R13$ (pot.)	= 220 Ω	$R38$	= 39 k
$C2$, 4	= 120 pF	$R14$, 15 metal film	= 390 Ω	$R39$, 40, 41, 42	= 1 Ω/ 1 W
$C3$, 5, 7, 9, 11, 13, 15	= 0.1 μF			$R43$	= 180 Ω.
$C6$	= 1.5 nF	$R16$, 17	= 1.8 k		
$C8$, 10, 12, 14	= 0.68 μF	$R18$, 19, 21, 22 metal film	= 100 Ω		
$D1$	= BZY88C10				
$D3$	= BZY88C13	$R20$	= 560 Ω/1 W.		
$D2$, 4, 5	= BA145				
$L1$	= 2 μH.				

Resistors $\frac{1}{4}$ W carbon film unless otherwise specified, small capacitors polystyrene, large capacitors polyester.

The Amplifier Design

The basic design philosophy is as follows.

1) First, to provide the required high open-loop linearity by using heavy local feedback in every amplifier stage. This minimizes the need for heavy overall feedback and at the same time increases the open-loop cutoff frequency of the amplifier.

2) The high-power stages are used in a grounded collector configuration in order to increase their frequency response and linearity.

3) Voltage drive is used in the crucial output and driver stages to force the transistors to operate with a cutoff frequency of almost f_T instead of f_β (that is usual in current drive designs), and to minimize the effect of β-nonlinearity.

4) Only lead compensation networks are used within the amplifier to compensate for the transfer function poles up to 1 MHz. This makes possible an unconditionally stable amplifier.

5) A complete dc-coupled design is used with the same amount of feedback for ac and dc. This eliminates the usual dynamic dc level shift problem that can cause severe unsymmetrical clipping of transient signals.

6) In all stages a completely symmetrical design is used without bypass or bootstrap capacitors. This significantly improves the amplifier clipping and overload characteristics, makes clipping recovery instant and avoids dc level shift problems, as frequently encountered in conventional design. Furthermore, it improves amplifier linearity especially at high frequencies, where the even harmonics usually become a prime source of distortion.

7) All stages are used in class A except the power transistors, which operate in class AB with a high quiescent current to provide most of the signal output power in class A. This totally eliminates crossover distortion and asymmetries in the critical low-power region.

The circuit diagram of the amplifier is shown in Fig. 1.

The value chosen for the overall feedback was 20 dB, and a closed-loop gain of 32 dB was required to make the input sensitivity -6 dBV (0.35 V_{rms}). The total open-loop gain was then divided as follows:

$$13 \text{ for } T_{1\text{-}2}, 3 \text{ for } T_{4\text{-}5}, \text{ and } 11 \text{ for } T_{7\text{-}8}$$

(measured differential in–differential out).

The three first poles of the transfer function occur at frequencies between 200 kHz and 1 MHz, and are lead compensated by C_4-R_{43}, C_2, and C_6. The total open-loop frequency response after lead-compensation has a -3 dB point at 1 MHz. The final 6 dB/octave rolloff is produced by lag compensation network C_1-R_6, which is situated outside the loop [4], [5]. The -3 dB point of this network is 100 kHz and the compensation is cut off at 1 MHz by R_6. As the open-loop cutoff frequency is above the audible frequency range, transient intermodulation distortion is not generated [1]. The phase margin of the feedback loop is greater than 80° at 1 MHz.

The amplifier is an inverting one with the same feedback value for ac and dc. Dc stability is ensured by using an input stage with a very good temperature stability. A dual transistor with an offset voltage drift of 3 μV/°C maximum is used for T_1 and T_2. With a maximum temperature excursion of ±50°C, the output offset voltage is below ±6 mV, which is negligible compared with normal output signals. Resistor R_{13} is to be adjusted for zero dc output voltage.

For a good linearity and a high cutoff frequency of the output stage, the bases of transistors T_{12} and T_{15} must be driven as symmetrical as possible and from a relatively low impedance. This is accomplished with transistors $T_{7\text{-}11}$ and $R_{18\text{-}27}$. Transistors T_7 and T_8 are a normal differential pair. T_9 and T_{10} form a current mirror circuit, familiar from integrated circuit technology. The current flowing through transistor T_{10} has the same amplitude as the current through transistor T_9. Therefore transistors T_8 and T_{10} perform current pumping in a symmetrical manner. The load for these two current sources is formed by a simulated Zener diode (T_{11}, R_{23}, R_{24}, and R_{25}) and two resistors (R_{26} and R_{27}). The simulated Zener diode keeps a constant bias voltage between the bases of T_{12} and T_{15}. The amplitude of the voltage swing on these two bases equals the current difference between T_8 and T_{10} times R_{36} and R_{27} in parallel. Transistors T_{12} and T_{15} are therefore driven from a symmetrical source with an impedance of 1.1 kΩ. Rather large emitter resistors R_{18}, R_{19}, R_{21}, and R_{22} are needed for good linearity, small gain, and linearization of unequalities in base–emitter voltages of the transistors $T_{7\text{-}10}$. This will give rather high voltage losses that would prevent the output stages from being driven over the full power supply range. The solution is to use second power supplies with higher voltages for the pre-stages. In this design ±30 V is used for the pre-stages and ±24 V for the output stages.

Transistors T_{12} and T_{15} work in class A. When the output transistors are driven in class B, and are switched off alternately, T_{12} and T_{15} remain conducting, so that the charge in the base–emitter junctions of the output transistors can easily flow away through the low output impedance of T_{12} and T_{15}. As a result the switching behavior of the output transistors is very good.

The quiescent current in the output stage is 600 mA. With 4 Ω load, class A operation is extended to about 3 W output power. This is 13 dB below the maximum rated output power, fulfilling adequately the requirement of having the amplifier for most of the signal time in class A [11].

The output transistors are cheap plastic-package types BD 203 and BD 204 ($f_\beta > 25$ kHz, $f_T > 3$ MHz). For power dissipation reasons, two of each are connected in parallel.

The high-frequency transients in the supply lines are suppressed with capacitors $C_{8\text{-}15}$. This suppression is aided by placing damping resistors ($R_{39\text{-}42}$) in series with some of the capacitors. The resulting resonant circuits formed by the supply line inductances and the capacitor-resistor networks are overcritically damped.

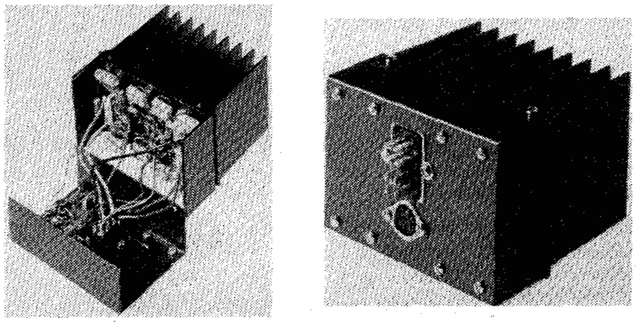
The amplifier short-circuit and overload protection circuit is a conventional two-transistor network between the power transistors and the driver bases. To make the circuit diagram clearer, this protection circuit is not shown in Fig. 1.

Mechanical Construction

The mechanical construction of the amplifier is shown in Fig. 2. The components are directly mounted on the heatsink, which has 0.75°C/W thermal resistance to the ambient. The amplifier quiescent power dissipation is 31 W and the maximum class AB total power dissipation is 60 W. The thermal stability is excellent, and because of the relatively high quiescent power dissipation the transistor junction temperature variation is rather small in operation.

Measurements

A survey of the measurement results is given in Table I. Amplifier small-signal frequency and phase responses are shown in Fig. 3. The -3 dB point is 1 MHz, at that frequency the phase shift is 100°. About 45° of this phase shift is caused by a first-order rolloff, and 55° by a propagation delay of approximately 150 ns. The frequency response is flat within -0.05 dB and the phase response within 3.5° in the frequency range 0–20 kHz.



(a) (b)

Fig. 2. The mechanical construction of the power amplifier. Transistors T_7–T_{17} are directly mounted on the heatsink, which has 0.75°C/W thermal resistance to the ambient. The maximum total power dissipation is about 60 W. The input stages are placed on a small printed circuit board which is mounted in the cover. Amplifier dimensions are 7.5 × 11.7 × 12.0 cm.

TABLE I
Survey of the Measurement Results

Rated output power	50 W_{rms}
Nominal load impedance	4 Ω
Output impedance	50 mΩ for 1 kHz 70 mΩ for 20 kHz
Damping factor	better than 50
Input impedance	3400 Ω
Input sensitivity	0.35 V_{rms} for rated output power
Feedback value	20 dB
Small-signal frequency responses	
open-loop 100 kHz	3 dB
closed-loop 0–20 kHz	flat within 0.05 dB
closed-loop 1.0 MHz	−3 dB
Power bandwidth for 0.2 percent harmonic distortion	35 kHz
Phase characteristic 0–20 kHz	flat within 3.5°
Slew rate	100 V/μs
Quiescent current (output stages)	0.6 A
Class A to B crossover point (4 Ω load)	2.9 W
Harmonic distortion, 1 kHz, 50 W	<0.2 percent
Intermodulation distortion, 7 kHz/250 Kz (1:4) for 25 W power level of the 250 Hz component	<0.15 percent
Noise level	106 dB (A) below full rated output power.

All measurements were done with short-circuited L_1.

The power bandwidth is shown in Fig. 4 for different criteria. With the usually employed criterion of visual clipping, the amplifier has a power bandwidth of 500 kHz. With the criterion of 0.2 percent total harmonic distortion proposed by us, the power bandwidth becomes 35 kHz, which is just sufficient for a signal source upper cutoff frequency of, say, 30 kHz.

The harmonic distortion is shown in Fig. 5 for different frequencies. As can be seen, the distortion at low-power levels for frequencies up to 10 kHz is infinitesimally small. No traces of crossover distortion can be found due to class A operation. The distortion figures up to 30 kHz are exceedingly good, especially when they are obtained with only 20 dB overall feedback. To measure the extremely small distortion values a HP3590A waveform analyzer was used, and the signal source was a Philips PM5125 signal generator followed by a Wandel and Golterman $\frac{1}{3}$-octave filter bank. The same setup was used to measure the intermodulation distortion, which was below 0.15 percent up to maximum output power of the amplifier. The test signals used were 7 kHz and 250 Hz in the ratio 1:4.

Fig. 6(a) and (b) show the square-wave responses at 1 and 100 kHz, clearly demonstrating the good

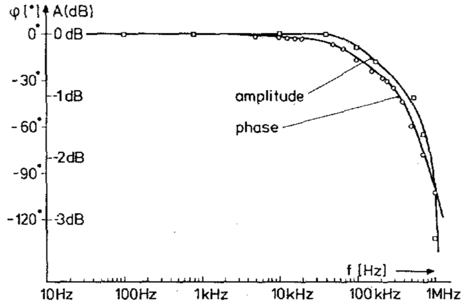


Fig. 3. Amplifier small-signal frequency and phase responses. The −3 dB point is 1 MHz. At this frequency the phase shift is 100°. About 45° is caused by a first-order rolloff, and 55° by a propagation delay of approximately 150 ns.

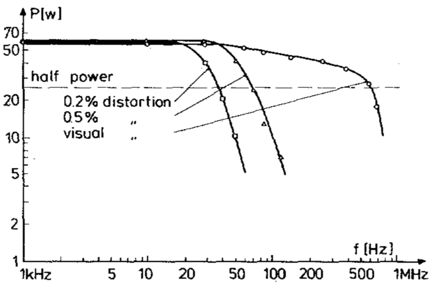


Fig. 4. Equidistortion curves: power versus frequency for three different criteria. For the proposed criterion of 0.2 percent total harmonic distortion the amplifier has a power bandwidth of 35 kHz (half-power point).

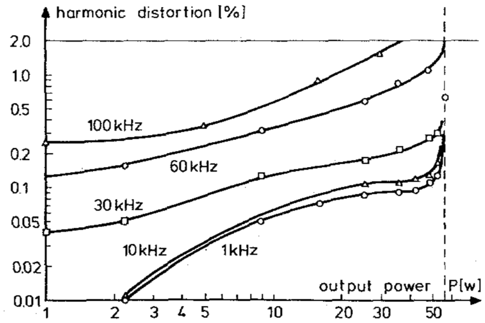
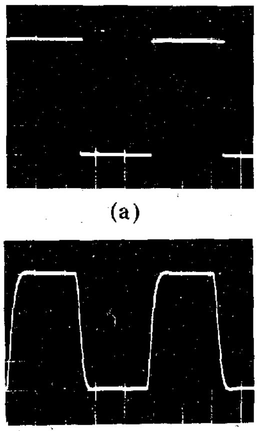


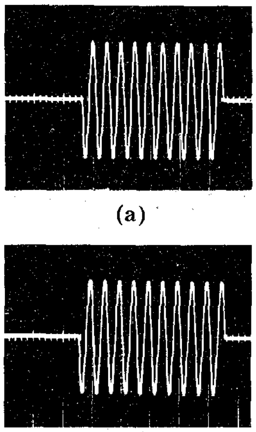
Fig. 5. Total harmonic distortion as a function of power for different frequencies. The distortion at low power levels for frequencies up to 10 kHz is infinitesimally small. No traces of crossover distortion can be found due to class A operation in the low power range.



(a)

(b)

Fig. 6. (a) Amplifier square-wave response at 1 kHz, 20 V peak-to-peak output, 4 Ω load. Horizontal: 200 μs/div. Vertical: 5 V/div. (b) Amplifier square-wave response at 100 kHz, 20 V peak-to-peak output, 4 Ω load. Horizontal: 2 μs/div. Vertical: 5 V/div.



(a)

(b)

Fig. 7. (a) Burst-tone test for 1 kHz sinusoidal burst, 20 V peak-to-peak output, 4 Ω load. Horizontal: 2 ms/div. Vertical: 5 V/div. (b) Burst-tone test for 100 kHz sinusoidal burst, 20 V peak-to-peak output, 4 Ω load. Horizontal: 20 μs/div. Vertical: 5 V/div.

amplitude and phase linearity and the unconditional stability of the amplifier.

When used in conjunction with a preamplifier having an upper cutoff frequency of 60-kHz maximum, the amplifier produces no internal transient overshoots and consequently does not exhibit transient intermodulation distortion at all.

Fig. 7(a) and (b) show a burst-tone test for frequencies of 1 and 100 kHz, respectively. The results are faultless.

All these measurements were done with short-circuited L_1. Even then the amplifier is unconditionally stable for capacitive loading up to 10 μF (maximum tested).

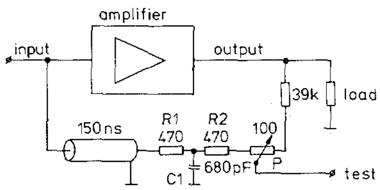


Fig. 8. Compensation test. Because the amplifier is an inverting one, a position can be found of potentiometer P where the linear component of the output signal exactly compensates the input signal at the "test" point. The momentary discrepancy signal, as scaled up to the output level, was below 0.01 percent for powers below 5 W and for frequencies in the audio range, and was mainly caused by incomplete phase compensation (R_1, R_2 and C_1).

A compensation test as in Fig. 8 was also performed. Because the amplifier is an inverting one, a position of potentiometer P can be found where the linear component of the output signal exactly compensates the input signal at the "test" point. The resulting signal at the "test" point then shows the total discrepancy between the input and the output signals. This momentary discrepancy signal, as scaled up to the output level, was below 0.01 percent for powers below 5 W and for frequencies in the audio range, and was mainly caused by incomplete phase compensation (R_1, R_2 and C_1 in Fig. 8). Near clipping the maximum discrepancy was of the order of 0.1 percent, caused by class B asymmetries, and the previously mentioned incomplete phase compensation. Sinusoidal, noise, and music signals were tested.

Conclusions

Using available low-frequency audio power transistors it is possible to construct an audio amplifier exhibiting exceedingly good phase characteristics, sufficient power bandwidth, no transient intermodulation distortion, and vanishingly small harmonic and intermodulation distortion. The amplifier is free from usually employed circuit tricks, and because of its symmetrical design and the absence of large capacitors it should lend itself to partial integration. The price paid is a relatively high quiescent power dissipation and the use of four power supplies, but they should not constitute severe limitations to the applicability of the design in cases where ultimate quality is required.

Summarizing, the amplifier does not exhibit any known source of distortion, instability or undesired response, which would not be far below the psychoacoustical sensation threshold.

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On the Location of Zeros and a Reduction in the Number of Adds in a Digital Ladder Structure

RONALD E. CROCHIERE

Abstract—**A modification is proposed in the design of digital ladder structures, which have transmission zeros. This results in a reduction in the number of adds required in the structure. The location of the transmission zeros under coefficient rounding is then analyzed.**

There has been considerable interest recently in the design of digital filter structures that are modeled after *LC* analog ladder structures or unit element structures [1]-[3]. One difficulty is that these structures are more complex and require more adds than most conventional digital structures. It is shown here that when the implementation of the structure contains transfer function zeros a simplification can be made in the structure and a saving of one add per complex zero pair can be achieved. Also the allowed transfer function zero locations are determined when the filter coefficients are rounded to their nearest fixed-point binary representation.

In digital ladder structures, complex zeros can be realized by a digital simulation of a parallel *LC* circuit in series with the line, as shown in Fig. 1(a). They can be realized alternatively by digital simulation of a series *LC* circuit in shunt with the line, as shown in Fig. 1(b). The unit element realization of these circuits [1] can be obtained with the aid of the Richards transformation and Kuroda's identities [see Fig. 2(a) and (b)]. Finally, the digital realizations are obtained from the unit element circuits [see Fig. 3(a) and (b)].

For the case of the digital circuit in Fig. 3(a), the reflection factor $B(z)/A(z)$ can be determined as

$$\frac{B(z)}{A(z)} = -\frac{z^{-1}(z^{-1}+\alpha)}{1+\alpha z^{-1}}, \tag{1}$$

where

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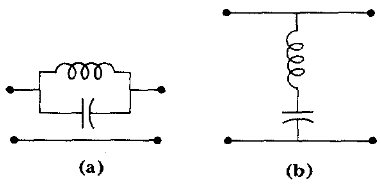

Fig. 1. (a) Parallel *LC* circuit in series with the line. (b) Series *LC* circuit in shunt with the line.

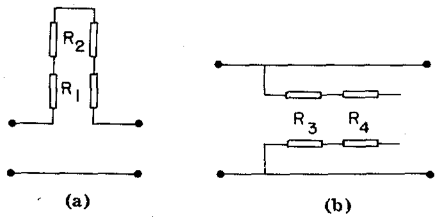

Fig. 2. (a) Unit element realization of circuit of Fig. 1(a). (b) Unit element realization of circuit of Fig. 1(b).

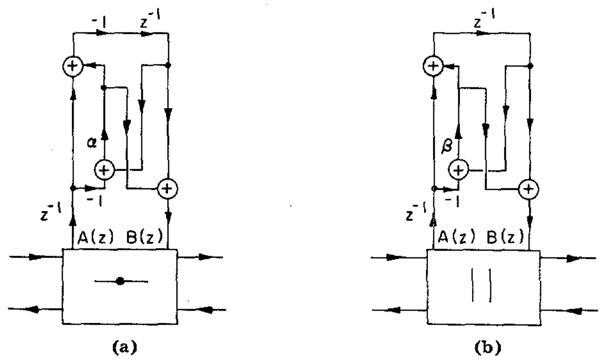

Fig. 3. (a) Digital realization of unit element circuit of Fig. 2(a). (b) Digital realization of unit element circuit of Fig. 2(b).

$$\alpha = \frac{R_1 - R_2}{R_1 + R_2}. \tag{2}$$

Similarly for the circuit in Fig. 3(b) the reflection factor is