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Nonlinear Effects of Radio-Frequency Interference in Operational Amplifiers

Franco Fiori and Paolo S. Crovetto

Abstract—In this brief, the susceptibility of operational amplifiers to radio frequency interference (RFI) is studied by a new analytical model. The proposed model, in particular, points out the dependence of the RFI induced dc offset voltage shift in operational amplifiers on design parameters and parasitics, giving both a good insight into the nonlinear mechanisms involved in the phenomenon and a support to integrated circuit designers in order to develop high immunity operational amplifiers. The validity of the proposed approach is discussed comparing model predictions with the results of computer simulations and experimental measurements.

Index Terms—Electromagnetic compatibility (EMC), electromagnetic interference (EMI), harmonic distortion, operational amplifier.

I. INTRODUCTION

The increased level of environmental electromagnetic pollution makes mandatory the design of electronic systems which are immune to radio frequency interference (RFI). In fact, metal interconnections (wires and printed circuit board traces) of electronic systems translate electromagnetic interference (EMI) into voltages and currents, which result superimposed on nominal system signals. Such an interference reaches integrated circuit (IC) terminals and drives distortion phenomena in active nonlinear devices, generating temporary or definitive errors in IC and electronic system operations [1]–[3].

Analog circuits are particularly susceptible to RFI, as they lack the regenerative effect which is typical of digital circuits. This is one of the main reasons why digital signal processing is preferable to analog signal processing. However, analog signal processing cannot be replaced in many applications, among which at least the analog-to-digital (A/D) and the digital-to-analog (D/A) conversions must be cited, which are necessary in digital signal processing because of the intrinsically analog nature of the information in the physical world. Among analog circuits, operational amplifiers (opamps) are extremely susceptible to RF disturbances. They demodulate RFI added on nominal input signals and so the nominal output signal is corrupted by in-band interference. In particular, the presence of continuous-wave (CW) interference generates an output offset voltage.

This opamp behavior was originally observed in aeronautic electronic systems and subsequently studied performing immunity tests on commercial opamps. In particular, measurements of the output offset voltage induced by RFI conveyed on the input terminals of several feedback opamps were performed varying interference frequency and amplitude [4]. These experimental characterization is useful in the design of EMI filters. More recently, this behavior has been studied by time domain [5]–[7] and frequency domain (harmonic balance) [8] computer simulations: several efforts have been expended on research in order to derive both RFI-oriented numerical models of active devices and opamp macromodels intended to reduce computer simulation time. Although these models allow one to predict efficiently and accurately the RFI-induced upset in opamps, they do not grant a relationship with circuit parameters and parasitics and so they cannot be directly applied to derive design criteria.

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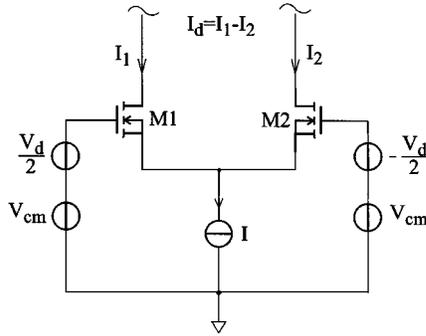


Fig. 1. nMOS differential pair.

This paper shows that RFI demodulation in feedback opamps is due to distortion phenomena in the input differential pair and presents a new approximate analytical model of the RFI induced dc offset shift. This model, which can be useful in order to derive high immunity design criteria for opamps, also gives a good insight into the nonlinear mechanisms involved in the phenomenon and gives an explanation about the generation of even-order distortion in differential pairs.

II. NONLINEAR OPERATION OF MOS AND BJT DIFFERENTIAL PAIRS

The work presented in this brief refers to common opamps composed of a cascade of amplifying stages the first of which includes a differential pair. RFI superimposed on the opamp input signals is considered and its frequency is assumed to be significantly higher than the cutoff frequency of the first stage. This assumption restricts the application of the model presented in the following to opamps employed in the elaboration of base-band signals and limits the analysis of distortion phenomena to the input differential stage. Besides, upsets induced by RFI in the quiescent operating point of the first opamp stage are amplified by the low frequency gain of the following stages and induce output signal upsets of considerable amplitude.

In the following parts of this brief, it is shown that the non linear operation of a differential pair driven simultaneously by common mode and differential mode interference generates demodulated RFI, which is superimposed on the nominal output signal of the differential pair. The specific case of CW RFI superimposed on the nominal input signals is considered and the upset induced in quiescent operating point is analytically evaluated.

The differential pair, as shown in Fig. 1, is made up of two source coupled n-channel MOS transistors biased by a current source I . It acts as a differential transconductance amplifier, i.e., its input signal is the difference between the voltages at its input terminals (the differential voltage, V_d) and its output signal is the difference between the drain currents of the transistors $I_d = I_1 - I_2$. Assuming that both transistors are biased in the saturation region, a simplified nonlinear static expression for the differential current is derived

$$I_d = \begin{cases} -I, & V_d \leq -\sqrt{\frac{I}{\beta}} \\ V_d \sqrt{2\beta I} \sqrt{1 - \frac{\beta V_d^2}{2I}}, & |V_d| \leq \sqrt{\frac{I}{\beta}} \\ I, & V_d \geq \sqrt{\frac{I}{\beta}} \end{cases} \quad (1)$$

where I is the bias current of the differential pair and

$$\beta = \frac{\mu C_{ox}}{2} \frac{W}{L}$$

where μ is the mobility of electrons (holes) in nMOS (pMOS) devices, C_{ox} is the capacitance of the gate oxide per unit of area W and L

are respectively the width and the length of the gate area of the MOS devices of the pair.

Expression (1) is usually regarded as a function of only the variable V_d , as β and I are assumed to be constant design parameters. Based on this assumption, even-order distortion and in particular dc offset shift cannot be experienced in the output differential current since I_d is expressed by (1) as an odd function of V_d [9]. In the case of simultaneous fluctuations of the bias current I and of the differential voltage V_d , the output differential current includes even-order spectral components. This fact is pointed out when performing the second order series expansion of (1) for $V_d = 0$, $I = I_0$ and V_{cm} within the input stage common mode dynamic range. The general series expansion of (1) is expressed by

$$I_d^{(2)} = I_d|_{0,I_0} + \left. \frac{\partial I_d}{\partial V_d} \right|_{0,I_0} v_d + \left. \frac{\partial I_d}{\partial I} \right|_{0,I_0} i + \frac{1}{2} \left. \frac{\partial^2 I_d}{\partial V_d^2} \right|_{0,I_0} v_d^2 + \frac{1}{2} \left. \frac{\partial^2 I_d}{\partial I^2} \right|_{0,I_0} i^2 + \left. \frac{\partial^2 I_d}{\partial V_d \partial I} \right|_{0,I_0} v_d i \quad (2)$$

where the small letters indicate the small signal component of the quantities defined before.

Given that

$$\begin{aligned} I_d|_{0,I_0} &= 0 \\ \left. \frac{\partial I_d}{\partial V_d} \right|_{0,I_0} &= g_m = \sqrt{2\beta I_0} \\ \left. \frac{\partial I_d}{\partial I} \right|_{0,I_0} &= 0 \\ \frac{1}{2} \left. \frac{\partial^2 I_d}{\partial V_d^2} \right|_{0,I_0} &= 0 \\ \frac{1}{2} \left. \frac{\partial^2 I_d}{\partial I^2} \right|_{0,I_0} &= 0 \\ \left. \frac{\partial^2 I_d}{\partial V_d \partial I} \right|_{0,I_0} &= g_p = \sqrt{\frac{\beta}{2I_0}} \end{aligned} \quad (3)$$

Equation (2) can be written as

$$I_d^{(2)} = g_m v_d + g_p v_d i. \quad (4)$$

In (4) it can be noted how the differential current actually depends both on v_d and on the product $v_d i$. This phenomenon is usefully exploited, for example, in RF mixer circuits.

Equation (4) is still valid for BJT differential pairs. In this case the differential current is given by

$$I_d = \alpha_F I \tanh\left(\frac{V_d}{2V_T}\right) \quad (5)$$

and the coefficients of the series expansion are

$$\begin{aligned} I_d|_{0,I_0} &= 0 \\ \left. \frac{\partial I_d}{\partial V_d} \right|_{0,I_0} &= g_m = \frac{\alpha_F I_0}{4V_T} \\ \left. \frac{\partial I_d}{\partial I} \right|_{0,I_0} &= 0 \\ \frac{1}{2} \left. \frac{\partial^2 I_d}{\partial V_d^2} \right|_{0,I_0} &= 0 \\ \frac{1}{2} \left. \frac{\partial^2 I_d}{\partial I^2} \right|_{0,I_0} &= 0 \\ \left. \frac{\partial^2 I_d}{\partial V_d \partial I} \right|_{0,I_0} &= g_p = \frac{\alpha_F}{4V_T}. \end{aligned} \quad (6)$$

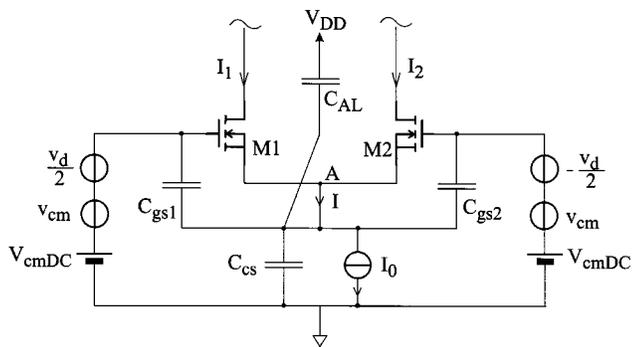


Fig. 2. nMOS differential pair including parasitic capacitances.

Referring to (4) it can be immediately observed that sinusoidal variations at the same frequency of the differential voltage and of the bias current generate a dc output-current offset shift. Furthermore, it should be noted that such a shift, as any kind of even order distortion in a differential pair [9], cannot be described without considering the overall bias current to be a variable, being (1) and (5) odd functions in the argument V_d .

III. RFI-INDUCED FLUCTUATIONS OF THE BIAS CURRENT

Although the bias current in a differential pair is intended to be fixed, common mode RF disturbances applied to the input terminals induce fluctuations on it because of the finite shunt admittance of the bias current source. If RF disturbances induce both differential and common mode RF components at the same frequency, as it is very common in practical cases, a dc shift in the differential current is experienced. This effect is pointed out in (4). The analysis of the nonlinear phenomena induced by RFI is performed referring to the circuit shown in Fig. 2. It includes common mode (v_{cm}) and differential mode (v_d) RFI voltage sources added to the dc intentional signal (V_{cmDC}). The intentional differential voltage is assumed to be zero. The capacitance C_{cs} represents the drain-body reverse junction of the biasing transistor of the differential pair (not shown in Fig. 2), while C_{gs1} and C_{gs2} are the gate-source capacitances of transistors M1 and M2 respectively.

The capacitance C_{AL} in the same figure is related to the reverse polarized isolation junction as shown in the twin-tub process cross section in Fig. 3(a). The parasitic capacitance C_{sb} plays the same role of C_{AL} if the p-well is directly tied to ground. A similar parasitic capacitance (C_{GND}) exists in p-MOS differential pairs as shown in Fig. 3(b).

The circuit in Fig. 2 has been analyzed in the frequency domain by using the small signal equivalent circuit shown in Fig. 4 and the following expression for the effective bias current $I(j\omega)$ is derived

$$I(j\omega) = g_m \frac{2j\omega C_T V_{cm}(j\omega) + j\omega (C_{gs2} - C_{gs1}) V_d(j\omega)}{j\omega (C_{gs1} + C_{gs2} + C_T) + 2g_m} \quad (7)$$

where

$$C_T = C_{cs} + C_{AL}$$

is the overall capacitance connected between node A and ac ground whereas $V_d(j\omega)$ and $V_{cm}(j\omega)$ are respectively the differential and the common mode component of the input voltage in the frequency domain, as shown in Fig. 4.

If the transistors of the differential pair are matched

$$C_{gs1} = C_{gs2} = C_{gs}$$

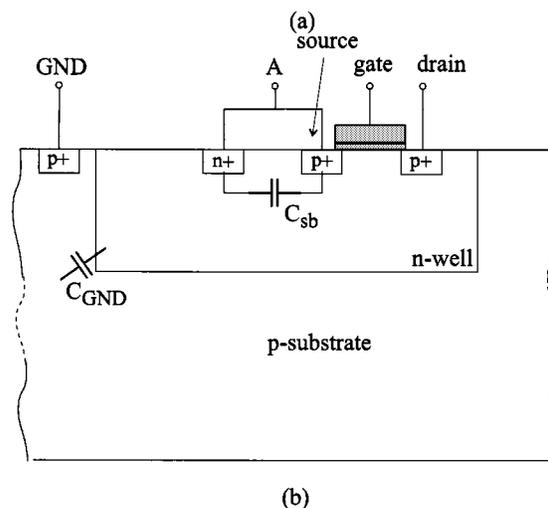
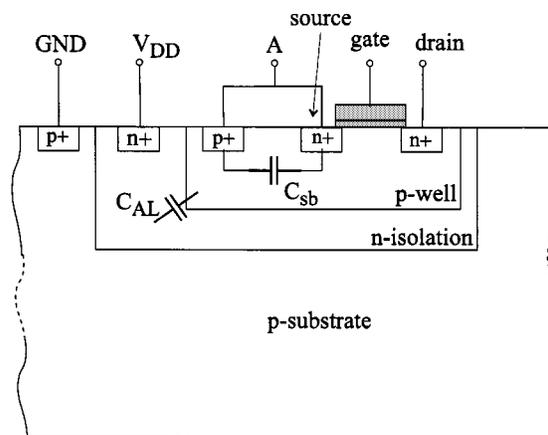


Fig. 3. Standard cross-section of a CMOS twin-tub process.

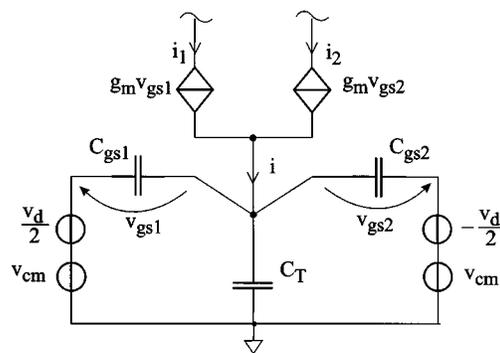


Fig. 4. Small-signal equivalent circuit of the differential pair.

and (7) can be written as

$$I(j\omega) = V_{cm}(j\omega) \frac{2g_m j\omega C_T}{j\omega (2C_{gs} + C_T) + 2g_m} = V_{cm}(j\omega) Y(j\omega). \quad (8)$$

Equation (8) points out how the common mode component of the input voltage induces RF fluctuations in the effective bias current of the input transistors.

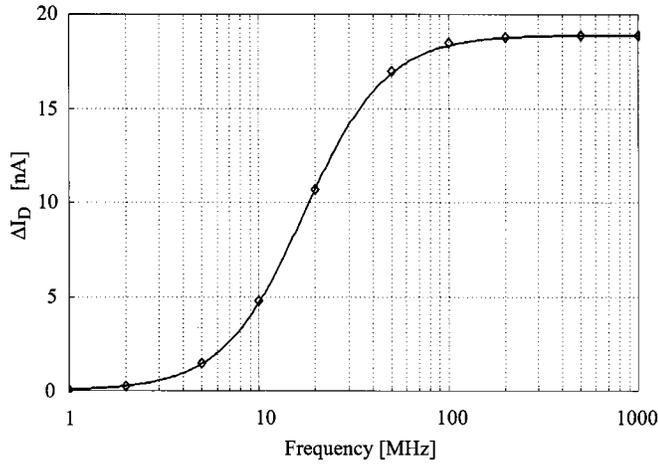


Fig. 5. Differential-current dc offset shift (ΔI_D) versus frequency.

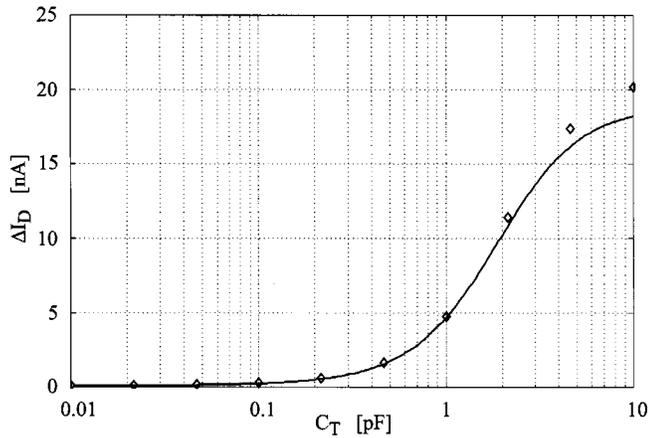


Fig. 6. Differential-current dc offset shift (ΔI_D) versus capacitance (C_T).

IV. EVALUATION OF THE RFI-INDUCED DIFFERENTIAL-CURRENT SHIFT

Once one has computed the bias current fluctuations as a function of the common mode and differential mode input interference, the output current offset shift is obtained by using (4). This approach can be proven to be equivalent to Volterra series method for the analysis of nonlinear systems, in particular to its circuit theory formulation given in [10] and [11], therefore it is very accurate for small amplitude interference and still gives good results as long as no transistor is driven out of its correct region of operation (saturation region for MOS transistors, forward active region for bipolar transistors).

If the differential mode and the common mode voltage fluctuations are expressed by

$$\begin{aligned} v_d &= V_{d,\text{pk}} \cos(\omega t) \\ v_{\text{cm}} &= V_{\text{cm},\text{pk}} \cos(\omega t + \varphi_{\text{cm}}) \end{aligned}$$

the effective bias current fluctuations can be derived performing the inverse-Fourier transform of (7), hence

$$i(t) = \mathcal{F}^{-1}[I(j\omega)] = |I(j\omega)| \cos(\omega t + \angle I(j\omega)). \quad (9)$$

Then, the output differential current is derived from (4)

$$i_d = g_m V_{d,\text{pk}} \cos(\omega t) + g_p V_{d,\text{pk}} \cos(\omega t) |I(j\omega)| \cos(\omega t + \angle I(j\omega)) \quad (10)$$

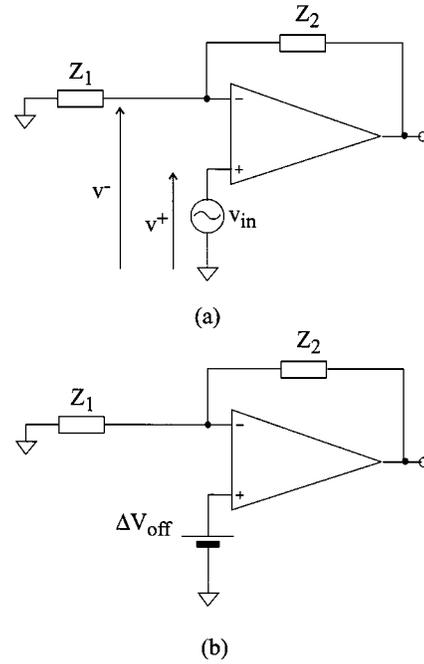


Fig. 7. (a) A feedback opamp with RFI (v_{in}) applied to the noninverting input. (b) Equivalent circuit of a feedback opamp subjected to RFI. The input offset voltage source ΔV_{off} represents the effects of RFI in opamp.

and finally the output offset current induced by RFI distortion in the input differential pair is expressed as

$$\Delta I_D = \frac{g_p V_{d,\text{pk}} |I(j\omega)|}{2} \cos(\angle I(j\omega)) \quad (11)$$

or, using (8), as

$$\Delta I_D = \frac{g_p V_{d,\text{pk}} V_{\text{cm},\text{pk}} |Y(j\omega)|}{2} \cos(\varphi_{\text{cm}} + \angle Y(j\omega)). \quad (12)$$

This expression highlights how the dc current shift depends on the product of the amplitudes of the differential and of the common mode voltages. This fact is in perfect agreement with computer simulations which show no offset shift but when both a common mode and a differential mode RF component on the input terminals are applied.

The prediction of the proposed model of the differential pair is compared with the results of computer simulations performed with the SPICE-like simulator ELDO [12] using the models of the devices available in the $1 \mu\text{m}$ BCD3s technology process [13]. Fig. 5 shows the predicted (continuous line) and the simulated (diamonds) dc differential current shift versus frequency in the case of $V_{d,\text{pk}} = V_{\text{cm},\text{pk}} = 10 \text{ mV}$. In the proposed simulation, the stage is biased by an ideal current source $I_0 = 10 \mu\text{A}$ and a parallel capacitance $C_T = 1 \text{ pF}$ is added in order to take into account the parasitic well capacitance, which is not considered in transistor models. The β parameter of the input devices is derived from the operating point dc analysis performed by ELDO. The dependence of the RFI behavior of the differential pair on the well parasitic capacitance C_T is shown in Fig. 6.

V. RFI-INDUCED INPUT OFFSET VOLTAGE SHIFT IN FEEDBACK CONFIGURATIONS

The proposed approach can be directly applied in order to predict the RFI effects in feedback opamp circuits.

A. Analytical Approach

This kind of analysis has to be carried out in three steps:

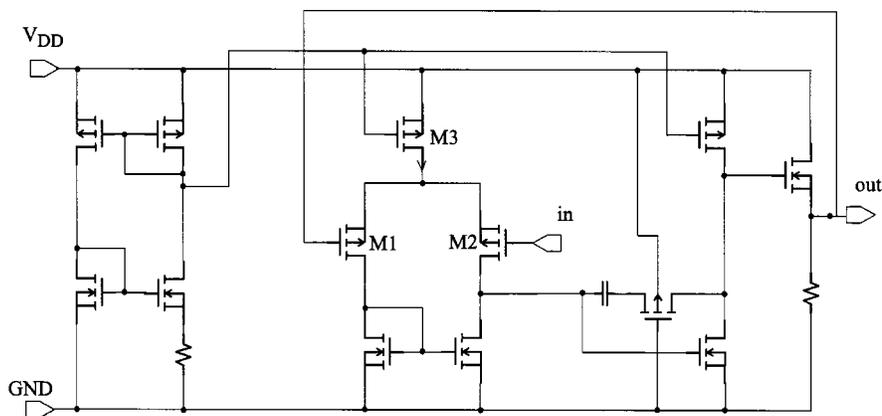


Fig. 8. Two-stage operational amplifier in the voltage follower configuration.

- evaluation of the input common mode and differential mode voltages in the feedback configuration as a function of the RF disturbances on the external input;
- use of the previously discussed model in order to derive the dc differential current shift in the input differential pair;
- evaluation of the input offset voltage, dividing the differential current offset by the input stage differential transconductance.

In the general case, the common mode and differential mode input voltages can be expressed as a function of the RF input signal if one knows all circuit elements, the opamp differential amplification and the common mode rejection ratio as transfer functions in the frequency domain. However, if the interference frequency is significantly higher than the opamp first stage cutoff frequency, the amplitude of RF signal superimposed on the opamp output nominal signal and fed back to the inverting input is negligible. As a consequence, the differential and the common-mode voltages can be easily derived as a function of the input interfering signal. For instance, the opamp in the circuit in Fig. 7(a) is excited by an RF voltage source v_{in} , hence the non inverting RF input voltage v^+ is equal to v_{in} , the inverting input RF voltage v^- is about zero and the common mode and the differential mode voltages become, respectively, $v_{cm} \simeq v_{in}/2$, and $v_d \simeq v_{in}$. If one substitutes the obtained voltages in (11), the dc shift in the differential current is evaluated. At this point, as it is usually done in order to compute the input offset voltage due to transistor mismatch, the RFI induced input offset voltage shift is evaluated dividing the dc differential current shift by the differential transconductance of the first stage

$$\Delta V_{\text{off}} = \frac{\Delta I_D}{g_m}. \quad (13)$$

In this way, the RFI effects in a feedback opamp are described by an input offset voltage source and consequently the circuit in Fig. 7(a) is equivalent to that shown in Fig. 7(b). Such an equivalence allows one to predict RFI effects in circuits which includes opamps by performing low-frequency-time-domain analysis.

B. Computer Simulation and Experimental Measurement Results

The proposed approach has been validated by considering the two-stage opamp [14] reported in Fig. 8, connected in the voltage follower configuration. This circuit has been designed referring to the $1 \mu\text{m}$ BCD3s technology process and the upsets induced by CW RFI superimposed on the input nominal signal have been evaluated by performing time domain analysis with ELDO.

Furthermore, the CMOS Miller opamp has been fabricated (see Fig. 9) and experimentally characterized: measurements have been carried out on wafer employing the test bench illustrated in Fig. 10.

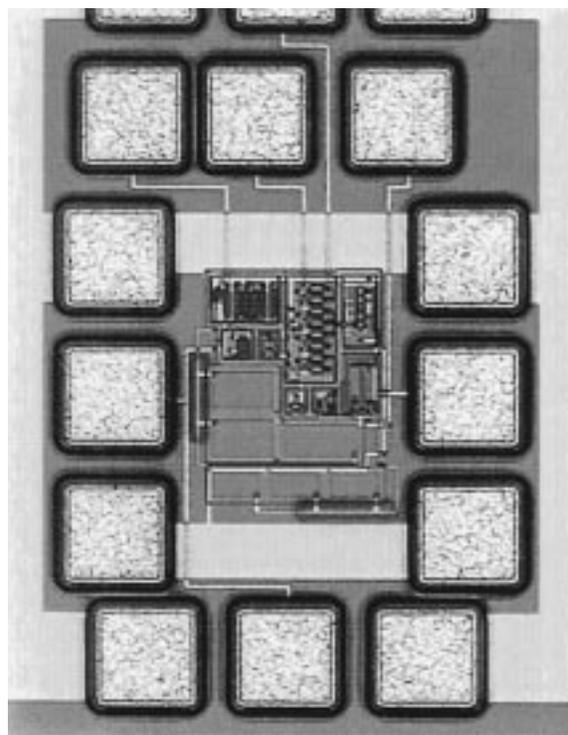


Fig. 9. Chip photography of the designed two-stage operational amplifier.

The input *ground-signal-ground* (GSG) pads of the opamp are contacted by an RF probe [15], which is connected to a bias tee: the dc input of the bias tee is connected to a constant voltage source V_{inDC} , while its RF input is connected to an RF source with impedance $R_L = 50 \Omega$, in order to add RF signals to the nominal dc input voltage V_{inDC} . The opamp output GSG pads are contacted by an RF probe which is connected to a bias tee as well: its dc port is connected to a dc voltmeter in order to measure the dc component of the output voltage while the RF port is connected to the load $R_L = 50 \Omega$. The dc power supply voltage (V_{DD}) for the amplifier is given by a 5-V dc voltage source.

The RFI-induced dc offset voltage shift has been measured comparing the dc output voltage obtained when the RF voltage source is turned off with the value measured when an RF signal is injected, for the same mid-range dc level of the input signal $V_{\text{inDC}} = 2.5 \text{ V}$.

A comparison of the dependence of the input offset voltage shift on the amplitude of the RF interference obtained from model prediction, time-domain computer simulation and experimental measurement has been carried out for different frequencies of the interfering signal. The

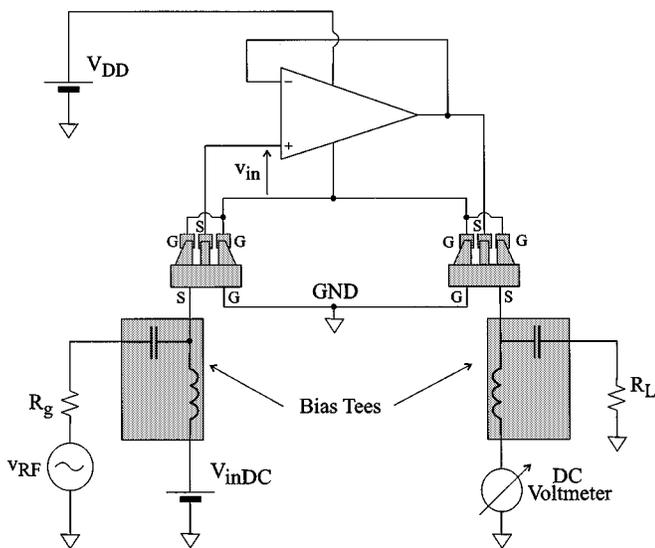


Fig. 10. Schematic view of the experimental test setup.

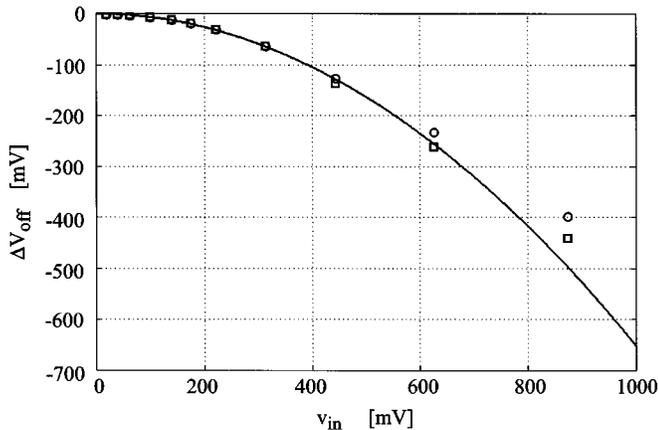


Fig. 11. Predicted (continuous line), simulated (squares) and measured (circles) RFI induced input offset voltage shift (ΔV_{off}) versus interference peak amplitude (v_{in}). The interference frequency is fixed to 100 MHz.

results obtained for a 100-MHz sinusoidal interfering signal are plotted in Fig. 11. In addition, measurements and simulations of the input offset voltage versus interference frequency have been carried out for a constant RFI amplitude. Measured (circles), simulated (squares) and predicted (continuous line) values are reported in Fig. 12. The agreement of model predictions, in which only the nonlinear behavior of the differential pair is considered, with the time domain computer simulations of the whole opamp together with the experimental measurements confirms the validity of the proposed model. Furthermore, it should be noted that the dc input offset voltage shift is almost frequency independent for frequencies above 100 MHz.

VI. CONCLUSIONS

In this brief, the main nonlinear mechanism responsible of the RFI-induced dc offset shift in MOS and BJT opamps has been discussed and a new simple analytical model has been proposed to predict this behavior. This model has been validated comparing its predictions with computer simulations and experimental measurement

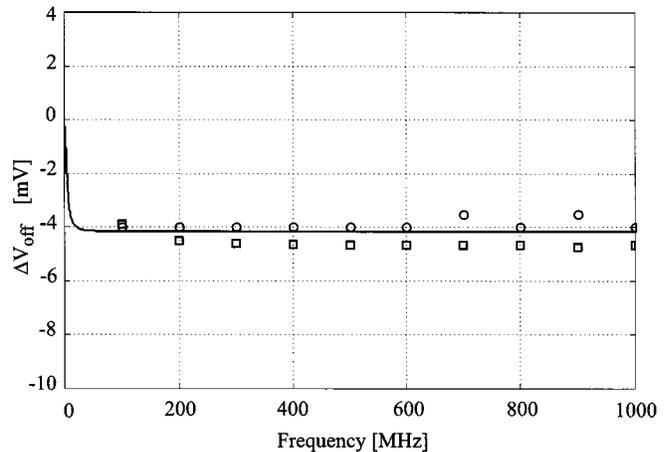


Fig. 12. Predicted (continuous line), simulated (squares) and measured (circles) RFI induced input offset voltage shift (ΔV_{off}) versus interference frequency. The interference amplitude is fixed to $|v_{\text{in}}| = 80$ mV.

results. This model also gives a rigorous explanation of the main cause of even-order distortion in integrated differential pairs.

Although this model is not suitable to study the behavior of opamps in the presence of very high amplitude disturbances, as it is based on the assumption that all the devices work in their nominal region of operation, it provides a good insight into the phenomenon and, especially, relates it to design parameters and parasitics. These features make the proposed approach suitable in order to derive low RFI design criteria and to develop new high immunity structures as well.

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