SESSION I: ANALOG TECHNIQUES

[See page 287 for Figure 5.]

WAM 1.4: A Quad CMOS Single-Supply Opamp with Rail-to-Rail Output Swing

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ALTHOUGH SPECIAL APPLICATION CMOS amplifiers are an accepted part of mixed analog/digital chips where their ability to be integrated outweighs their existing weaknesses, penetration into stand-alone applications has been limited to niches such as low voltage, very low power, and choppers. Unfortunately, problems in the input stage relating to input offset voltage, drift and noise, problems in the output stage driving realistic loads with adequate swing, problems obtaining high gain with such loads, and latch-up sensitivity have prevented CMOS from making a strong contribution to the mainstream amplifier arena. This paper will describe a CMOS amplifier that provides improved performance using a conventional 4μ, double polysilicon, P-well process optimized for digital chips.

The input stage is of a conventional topology (Figure 1), but has been optimized for performance. The high threshold Native P-channel device exhibits the least noise on most CMOS processes and has been chosen for the input pair, M1 and M2, while the mirror duties are performed by N-channels of substantially lower transconductance. Second stage transistor, M5, is biased such that the drain-to-source voltages of each input device pair are equal regardless of supply, load or temperature. The Natives are deliberately operated in their quasi-subthreshold region where they exhibit superior noise and match relative to the square-law region. The layout of the entire input stage (Figure 5) follows the die centerline of minimum surface stress as do the output stage power devices. M1 and M2 consist of 16 separate doughnut shaped geometries densely packed into a checkerboard pattern split by the centerline. M3 and M4 comprise a common-centroid cross-coupled quad also split by the centerline. These layout efforts contribute to the cancellation of processing gradients, thermal gradients, and package stress resulting in upgraded offset voltage distributions; Figure 2.

The output stage (Figure 3) is actually the integrator portion of the amplifier. It consists of an initial feed-forward stage driving a feed-forward, power push-pull final stage. The initial feed-forward stage is comprised of devices M5, M19 and M20 with C_{FF} providing feed-forward compensation. This stage contributes a non-inverting gain of about 40dB and is largely responsible for the high voltage gain of the amplifier. The push-pull stage consists of a high transconductance driver, Q7, feeding the output sink device, M8, directly and the output source device, M9, via level shifters M10 and M11. The current sharing between these level shifters determines the conduction level of M9. An AB bias of 200μA is set by the area scaling of the currents from bias transistors, M16 and M24, and is thus under good control. During large signal swing, neither M8 nor M9 completely shut off, resulting in a smooth transition from sink to source. Crossover distortion at 10kHz is only 0.01% while driving 2kΩ with a gain of ten. There is ample allowance for large gate overdrive on M8 and M9 which allows the amplifier to drive 2kΩ and even 600Ω loads. On just a +5V supply, the output swings to 130mV of the positive rail and 110mV of the negative rail, while driving a capacitor coupled 2kΩ load. Driving 600Ω produces swings of 390mV and 300mV, respectively. The feed-forward compensation capacitors, C_F and C_{FF}, are driven by Q23. Under small signal conditions, this allows M8 and M9 to be virtually under the direct control of the input stage near the unity cross frequency, thus aiding the stability of the overall amplifier.

Well-controlled bias currents are not easily achieved in CMOS. Combining the need for positive TC (to moderate the change in transconductance with temperature), high Power Supply Rejection Ratio (PSRR), accuracy, repeatability, and low voltage operation is a significant design challenge. The solution is possible by employing substrate NPN transistors and equipping them with lateral collector elements. Two such devices, Q26 and Q27, are area ratioed and connected in bootstrap fashion as part of a feedback ΔVbe generator circuit; Figure 4. The highly repeatable ΔVbe potential is forced across the resistor type with the best control, the P+ source/drain. The resultant current is repeatable run to run and possesses a TC of about +3000 PPM. As the operating voltage of the entire quad varies from +5V to +15V, the bias circuit helps keep the quiescent current change down to typically 6%. The bias circuit itself operates down to 2V, while the amplifier typically works down to 3V.

All four amplifiers in the quad are essentially free from latch-up. This is due to careful chip layout as the process does not use epi and parasitic NPN Beta runs fairly high.

The amplifier is not limited to stand-alone duty. Because performance is largely derived from circuit design and layout techniques, it lends itself well for use on predominantly digital chips that could be designed on a variety of polysilicon CMOS processes including single-poly and/or N-well.

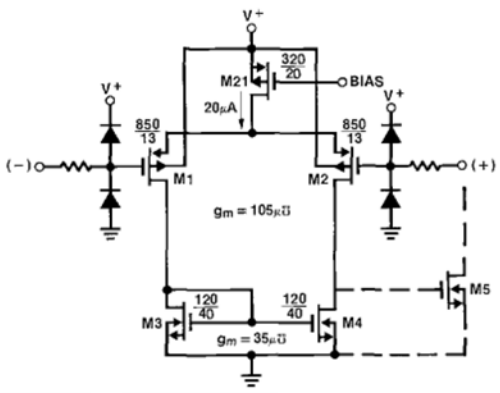

FIGURE 1—Input stage with common-mode voltage range that includes ground.

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