Lovoltech

Breakthrough Power JFET Technology

PWRLITE LD1107N

High Performance N-Channel Vertical *POWERJFET™* Transistor

Features

- Trench Power JFET with low threshold voltage Vth.
- Device fully "ON" with Vgs = 0.7V
- Optimum for "High Side" Buck Converters
- Optimized for Secondary Rectification in isolated DC-DC
- Low Rg and low Cds for high speed switching
- No "Body Diode"; extremely low Cds

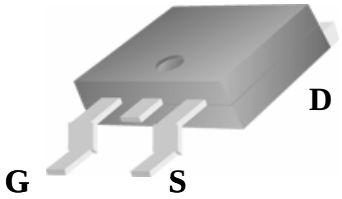
Applications

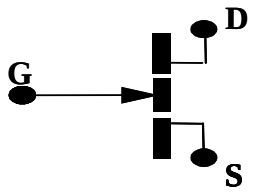
- VGA and Graphic Cards for stand-by operation
- DDR, SDRAM for stand-by operation Power Supply
- DC-DC Converters
- Synchronous Rectifiers
- PC Motherboard Converters
- Step-down power supplies
- Brick Modules
- VRM Modules

Description

The Power JFET transistor from Lovoltech is a device that presents a Low Rdson allowing for improved efficiencies in DC-DC switching applications. The device is designed with a low threshold such that drivers can operate at 5V, which reduces the driver power dissipation and increases the overall efficiency. Lower threshold produces faster turn-on/turn-off, which minimizes the required dead time. The transistor "No Body Diode" provides a very low associated parasitic capacitance Cds. Ringing is also reduced so that a lower voltage device may be a better solution.

DPAK Pin Assignments





Enhanced
N – Channel Power JFET

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	Gate	**Gate.** Transistor Gate
2	Drain	**Drain.** Transistor Drain
3	Source	**Source.** Transistor Source

Typical Product Summary		
V_{DS} (V)	Rdson (Ω)	I_D (A)
20V	0.008	15

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Units
Drain-Source Voltage	V_{DS}	15	V
Gate-Source Voltage	V_{GS}	-10	V
Gate-Drain Voltage	V_{GD}	-20	V
Continuous Drain Current	I_D	25	A
Pulsed Drain Current	I_D	40	A
Junction Temperature	T_J	-55 to 150°C	°C
Storage Temperature	T_{STG}	-65 to 150°C	°C
Lead Soldering Temperature, 10 seconds	T	260°C	°C
Power Dissipation (Derated at 25°C)	P_D	40	W

Thermal Resistance

Symbol	Parameter		DPAK Ratings		Units
$R\Theta_{JA}$	Thermal Resistance Junction-to-Ambient		60		°C/W
$R\Theta_{JC}$	Thermal Resistance Junction-to-Case		3		°C/W

Electrical Specifications

(T_A = +25°C, unless otherwise noted.)

The ϕ denotes a specification which apply over the full operating temperature range.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
	Static						
BV_{DSX}	Breakdown Voltage Drain to Source	I_D = 0.5 mA V_{GS}= 0 V		15	20		V
BV_{GDO}	Breakdown Voltage Gate to Drain	I_G = -50μA			-24	-20	V
BV_{GSO}	Breakdown Voltage Gate to Source	I_G = -50μA			-12	-10	V
$R_{DS(ON)}$)	Static Drain to Source[1] On Resistance (Current flows drain-to-source) See Fig. 1	I_G = 100 mA, I_D=+10A I_G = 40 mA, I_D=+10A			8 10	10 15	mΩ mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=0.1 V, I_D=250μA		250	380	450	mV
TC $V_{GS(TH)}$	Gate Threshold Voltage Temperature Coefficient				-2.7		mV/°C
	Dynamic						
Q_G	Total Gate Charge	ΔV_{Drive} =3V, I_D=10A,V_{DS}=15V			9		nC
Q_{GD}	Gate to Drain Charge	V_{DS} from 13.5V to 1.5V			4.4		nC
Q_{GS}	Gate to Source Charge	V_{GS} from -2.0V to +0.35V			3.4		nC
Q_{SW}	Switching Charge	V_{GS} from +0.35V to V_{DS} =1.5V			5.4		nC
R_G	Gate Resistance				2.0		Ω
$T_{D(ON)}$)	Turn-on Delay Time	V_{DD}=15V, I_D=15A V_{Drive} = 5 V Resistive Load			3.3		ns
T_R	Rise Time				14.4		
$T_{D(OFF)}$	Turn-off Delay						
T_F	Fall Time						
C_{ISS}	Input Capacitance	V_{DS}=10V, V_{GS}= -5 V, 1MHz.			1350		pF
C_{OSS}	Output Capacitance				270		
C_{GS}	Gate-Source Capacitance				1085		
$C_{GD=}C_{RSS}$	Gate-Drain Capacitance				270		
C_{DS}	Drain-Source Capacitance				5		

Notes:

1. Pulse width <= 500μs, duty cycle < = 2%

Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

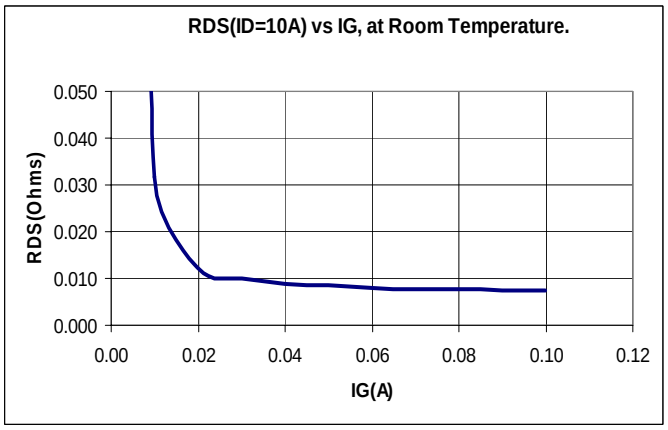


Figure 1 – R_{DSON} vs Gate Current at I_D – 10A

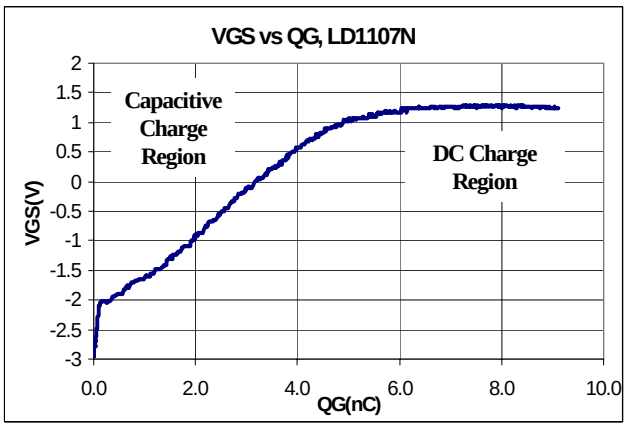


Figure 2 – Total Gate Charge

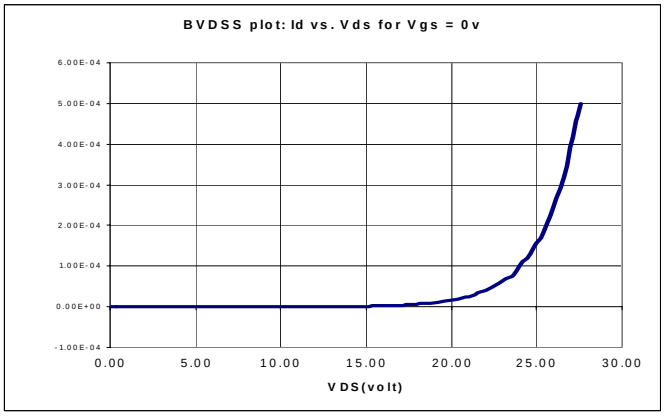


Figure 3 – Breakdown Voltage Vds vs Id

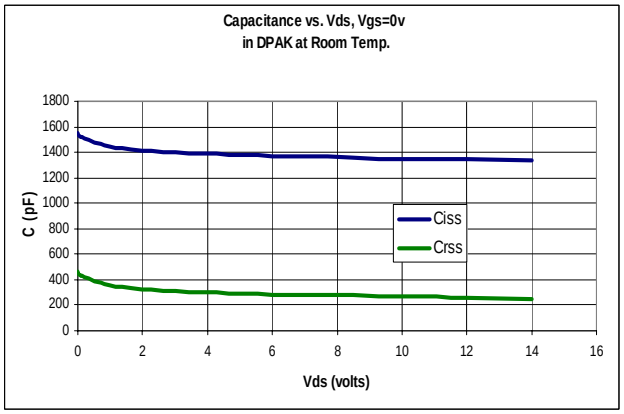


Figure 4 – Capacitance vs Drain Voltage Vds

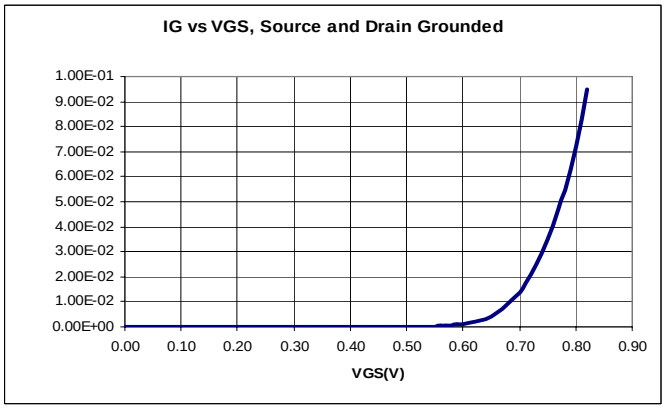


Figure 5 – I_G vs Gate Voltage V_{GS}

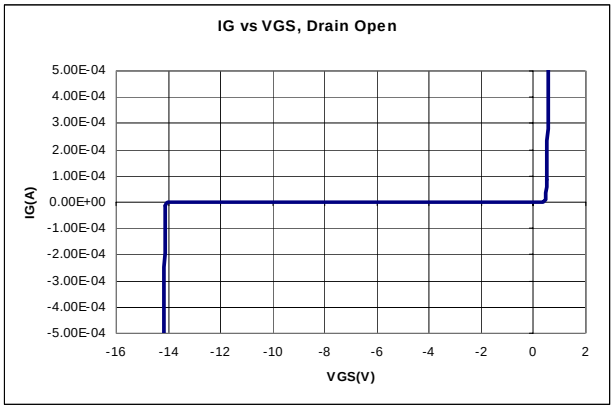


Figure 6 – Typical Gate Voltage Characteristic