A ltor A udio

JK-GEN 384-12

ERRATA SHEET

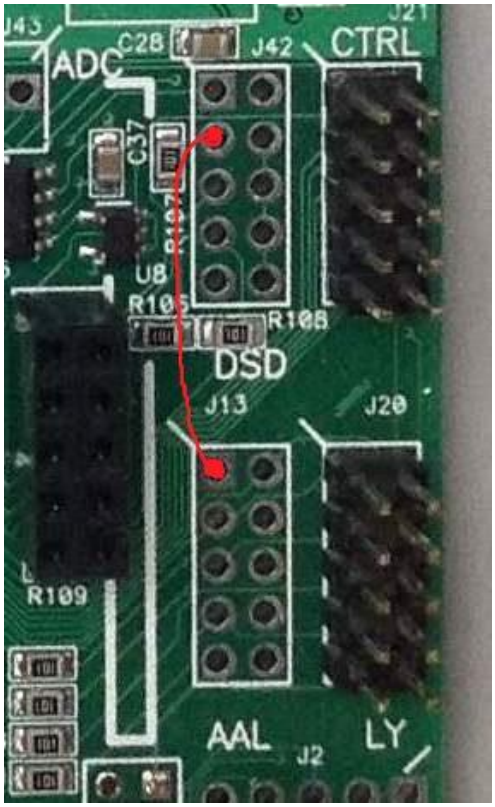
1. DSD MODE

Description:

PCB Version before 1.3a does not have DSD possibility.
Starting from PCB Ver. 1.3A DSD signals are present at I2S connector pins:
WCLK - > DSD_Left
SDATA -> DSD_Right
BCLK -> DSD_Clock

Workaround:

a) Check that resistors R107, R109 are exists, if not – put 100R 0805.
b) Connect with wire J42 pin 3 to J13 pin 1.



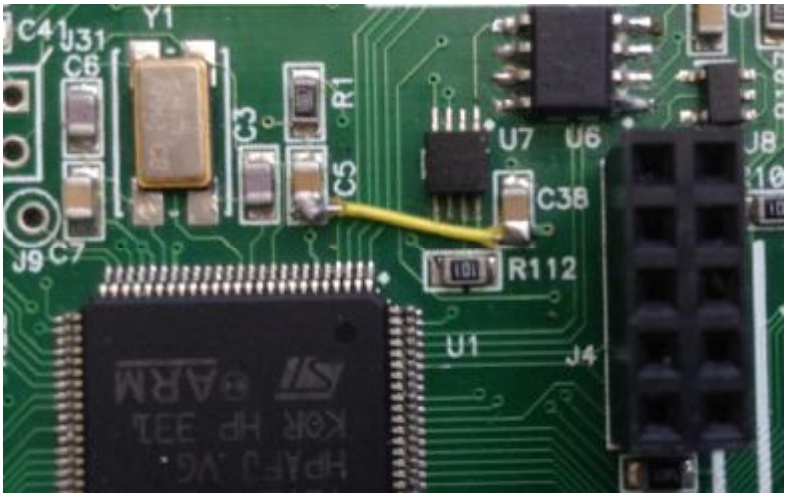
2. Internal MCLK is not always stable at 48/96/192/384 kHz.

Description:

Sometimes, the internal main clock is not stable at 48x sample rate scale.
. Actually for PCB Rev. 1.3 and 1.3a.

Workaround:

a) Open the case and check if the wire jumper exists:



If it exists – you do non need to do make anything. If it is not exists – continue.

b) Remove the Main PCB from the case
c) Cut wire at the bottom side, as shown on a picture below:

d) Put short wire on the top side, as it shown above.:

Remark: even if you do not observe the clock instability, it is highly recommended to do this modification.