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JITTER, JITTER, JITTER ...

Application Note AP-03

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1. INTRODUCTION

As the quality of analog-to-digital and digital-to-analog converters improves, jitter becomes an increasingly significant part of the signal imperfections in high-end and professional audio products. This application note presents a simple, yet mathematically correct, approach to jitter measurements and computations. It presents some of the most common causes of jitter, and illustrates jitter calculation methods with a concrete example. Finally, a jitter measurement system with a resolution of 1 ps is presented.

2. A DEFINITION OF JITTER BASED ON AUDIO PERFORMANCE

All electrical signals are analog in essence, even though the approximations "high" and "low" are quite convenient for digital signals. Clocks are no exception, and differ from their theoretical waveform both in voltage level and in timing. These voltage and time errors ultimately result in timing errors in the circuitry driven by the clock. A given set of imperfections on a clock signal produces different timing errors in different circuits, as they have different threshold, sensitivity to rise time, and so on. The following definition is proposed:

The jitter of a signal is the sequence of timing errors introduced in the receiving circuitry by the imperfections of this signal.

The receiving circuitry senses rising and falling edges of the incoming signal and the jitter is therefore defined as the sequence of timing errors on the rising and falling edges. In practice, however, only some of the edges are of interest. The output of a frequency divider / counter, for instance, is affected by only some of the edges of the incoming clock. All the edges are counted, but the timing of the output edges is sensitive to the timing of only some of the input clock edges, i.e. the edges causing the output to change. To be exact, the output timing also depends on the timing of the other edges, but their influence is very small and can usually be ignored. In the remainder of this document, the term "edge subset" refers to a set containing some or all of the rising and falling edges of a signal, presumably the ones influencing the performance of the product.

This in turn prompts a more useful definition of jitter involving edge subsets:

The jitter of a signal edge subset is the sequence of timing errors introduced in the receiving circuitry by the signal

edges belonging to the subset.

The timing error associated with the edge of rank k is denoted p(k). The jitter is the sequence { p(k) }.

In many cases, one wants to measure or compute jitter on edge subsets which are periodic. The edges are expected at times kT, (k = { $-\infty$, $+\infty$ }), and the corresponding timing errors are denoted { p(kT) }.

It will be shown in subsequent chapters that audio performance is affected by only some of the frequency components of the jitter. It is then natural to introduce the Fourier transform of the jitter { p(kT) }, which is defined as:

$$P(\omega) = \sum_{k=-\infty}^{\infty} p(kT)\, e^{-j\omega kT}$$

and its inverse transform, defined by:

$$p(kT) = \frac{T}{2\pi} \int_{-\frac{\pi}{T}}^{+\frac{\pi}{T}} P(\omega)\, e^{j\omega kT}\, d\omega$$

Some care must be exercised while computing $P(\omega)$ as the sum that defines it is not necessarily bounded.

Jitter is caused by components, starting with the clock, and as the signal progresses through the circuit, the jitter contribution of each individual stage is compounded with the jitter on its inputs to degrade the output timing. The compounding is a complex and often non-linear operation, but the following linear model is often a good approximation.

The linear model is characterized by two simplifying assumptions:

> The output jitter caused by input jitter is a linear function of the input jitter. The gain from input to output is defined as a complex function of the jitter frequency.
>
> The output jitter caused by the circuit itself is independent of the input jitter. The total output jitter is the sum of the jitters caused by the circuit and by the input jitter.

Let $H(\omega)$ be the circuit jitter transfer function, and let $P_i(\omega)$, $P_c(\omega)$ and $P_o(\omega)$ be the respective Fourier transforms of the input, circuit and output jitters: $p_i(kT)$, $p_c(kT)$ and $p_o(kT)$. The linear model states that:

$$P_o(\omega) = H(\omega)\, P_i(\omega) + P_c(\omega)$$

For example, the counter / divider mentioned above has a transfer function $H(\omega)$ equal to unity because each output edge is triggered by an input edge. The transfer function of a phase-lock loop circuit, on the other hand, is defined by its low-pass filter. Its magnitude is smaller than 1 for frequencies above its first pole.

This simple model can be used as a basis for the calculation of the total jitter caused by multiple sources. Jitter

variables and their transfer functions obey the same formalism as signals and filter transfer functions do.

Note: The assumption made earlier that the jitter caused by the circuitry is independent of the input jitter does not imply that it is independent of the input signal itself. In fact, for most circuits, the jitter depends heavily on the form of the input signal, as is shown in § 3.2.

3. MOST COMMON CAUSES OF JITTER

There are as many sources of jitter in a circuit as there are kinds of fish in the ocean, but the three sources outlined below are among the biggest fish.

3.1. NOISE

Analog noise on clocks and other signals is the primary source of jitter in many circuits.

The relation between noise and jitter is easily computed with the following first order approximation. Let dV/dt be the slope of the input signal around the input threshold of the receiving gate, and let n(k) be the noise voltage measured at the k th edge of the subset. The jitter p(k) is simply n(k) divided by dV/dt.

A similar relation can be established in the frequency domain. Each input edge acts as a sampling device which transforms the instantaneous voltage noise n(k) into a jitter p(k). Assuming the edges to be periodic and of period T, the sampling effect folds all the noise frequency components in the [-1/2T, +1/2T] interval. If $N(\omega)$ and $P(\omega)$ respectively represent the Fourier transforms of n(t) and p(kT) and are respectively defined on the intervals $(-\infty, +\infty)$ and $[-\pi/T, +\pi/T]$, they are linked by the following relation:

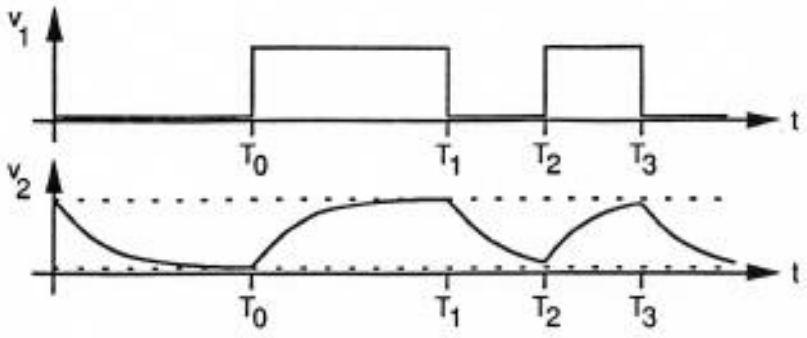
$$\frac{dV}{dt} P(\omega) = \sum_{m=-\infty}^{\infty} N\left(\omega + \frac{2\pi m}{T}\right)$$

Noise on the grounds and the power supplies produces similar effects by moving the gate threshold voltage. Because of the frequency folding caused by the sampling, even high frequency voltage noise can produce low frequency jitter.

3.2. ANALOG FILTERING OF COMPLEX DIGITAL SIGNALS

All digital signals go through some kind of analog filtering, be it a transmission line, the RC created by the impedance of an output driver and the printed circuit trace capacitance, or some other device. To periodic signals, such as clocks, analog filters only add the jitter described in 3.1. On complex signals, such as a transmission following the AES standard, analog filters add a considerable amount of jitter. A simple example illustrates this fact:

Let the ideal signal $v_1(t)$ presented in the next figure go through a one-pole RC filter to produce the signal $v_2(t)$, and let the input threshold of the receiver be halfway between the low and high levels V_l and V_h.



Between T_0 and T_1, the voltage $v_2(t)$ is defined by:

$$v_2(t) = V_h - (V_h - V_l)\, e^{-(t - T_0) / RC}$$

It crosses the threshold $(V_h + V_l) / 2$ at time $T_0 + RC \ln(2)$. In other words, the edge is delayed by $RC \ln(2)$.

The situation is different between T_2 and T_3, since $v_2(T_2)$ is not equal to V_l. The voltage v_2 is defined by:

$$v_2(t) = V_h - (V_h - v_2(T_2))\, e^{-(t - T_2) / RC}$$

It crosses the threshold at time $T_2 + RC \ln [\, 2 (V_h - v_2(T_2)) / (V_h - V_l) \,]$. This edge is delayed by $RC \ln [\, 2 (V_h - v_2(T_2)) / (V_h - V_l) \,]$ which differs from the delay previously calculated by:

$$\begin{aligned} \Delta t &= -RC \ln [\, (V_h - v_2(T_2)) / (V_h - V_l) \,] \\ &\approx -RC [\, (V_h - v_2(T_2)) / (V_h - V_l) - 1] \\ &\approx RC\, e^{-(T_2 - T_1) / RC} \end{aligned}$$

With $T_2 - T_1 = 160$ ns, and $RC = 40$ ns, which are values commonly encountered in AES transmitters and receivers, the difference Δt between the two delays is 733 ps. This number is the peak-to-peak value of the jitter introduced by the RC filter. It is clearly dependent on the input signal and cannot be regarded as a characteristic of the filter alone.

The large jitter mentioned above is unavoidable in the transmission of any digital data stream. Fortunately, the AES standard was so designed that almost all the jitter energy is concentrated at high frequencies, where it is most easily eliminated.

3.3. ANALOG SAMPLING CIRCUITS

Wherever digital-to-analog conversions occurs, there is a circuit defining the time at which the analog output changes its value. In digital-to-analog converters that possess a deglitcher, the deglitcher performs this function. In digital-to-analog converters that do not, the digital latch defines the transition time. In both cases the circuit may have some sensitivity to either the analog output level prior to the transition, or its level thereafter or both. The jitter caused by this sensitivity is correlated with the analog signal and produces characteristic signal degradations, as seen in § 4.2.

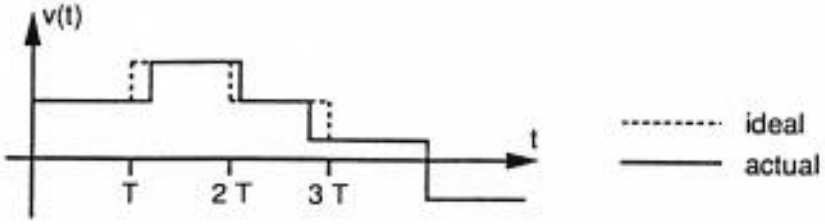
4. PERFORMANCE DEGRADATION CAUSED BY JITTER

Jitter eventually causes signal degradation. The case of audio oversampling digital-to-analog converters is examined, but similar degradation occurs in analog-to-digital converters. The following is an example of the application of jitter calculations, not a comprehensive treatment of digital-to-analog converters sensitivity to jitter.

4.1. OVERSAMPLING DIGITAL-TO-ANALOG CONVERTERS

Let a perfect converter convert digital data into an analog signal at a rate mF_S. F_S represents the sampling frequency (48 KHz for instance) and m is the oversampling multiplier (usually 4 or 8). Let $T = 1 / mF_S$.

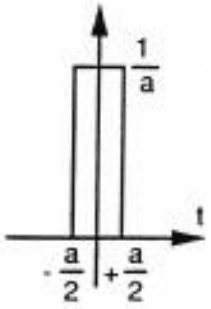
Ideally, the converter outputs the value v(kT) during the entire time interval [kT, (k+1)T]. However, jitter causes the output of the converter to change earlier or later than its due time kT, more specifically at time kT + p(kT).



If p(kT) is negative, the output changes earlier, causing an error v(kT) - v((k-1)T) during the interval [kT + p(kT), kT]. If p(kT) is positive, the output changes later than expected, causing an error equal to v((k-1)T) - v(kT) during the interval [kT, kT+p(kT)]. In both cases, since p(kT) is very small compared to T, the error can be approximated by a voltage impulse at time kT:

$$u(k, t) = p(kT) [v((k-1)T) - v(kT)] \delta(t-kT)$$

where $\delta(t)$ is the Dirac impulse function, defined as the limit of the following function when a approaches 0:



A Fourier transform is performed on the sum of the individual u(k, t):

$$U(\omega) = \sum_{k=-\infty}^{\infty} p(kT) [v((k-1)T) - v(kT)] e^{-j\omega kT}$$

It can be shown that the sum $U(\omega)$ is equal to the convolution product of $P(\omega)$ and $X(\omega)$, where $X(\omega)$ is the Fourier transform of the signal steps $x(kT) = v((k-1)T) - v(kT)$.

$$U(\omega) = \frac{T}{2\pi} \int_{-\frac{\pi}{T}}^{+\frac{\pi}{T}} X(\omega_1) P(\omega - \omega_1) \, d\omega_1$$

In other words, the spectrum of the error signal is the convolution product of the spectra of the signal steps and of the jitter. Since the signals are time-discrete, all frequencies referred to so far are modulo 1 / T.

Digital-to-analog converters are followed by a series of analog filters, including the speakers and the auditory organs of the listener. The portion of the error signal in the audio range [0, F_A = 20 kHz] can be retrieved from its Fourier transform:

$$u_F(t) = \frac{1}{2\pi} \int_{-2\pi F_A}^{+2\pi F_A} U(\omega) \, e^{j\omega t} \, d\omega$$

As an example, if both the signal steps and the jitter are sine waves of respective frequencies F_V and F_P, and amplitudes A_V and A_P, the error signal is the sum of two sine waves of frequencies $F_V + F_P$ and $F_V - F_P$, each with an amplitude $A_P A_V / 2\,T$. These frequencies may or may not fall in the audio band [0, F_A], depending on the signal frequency. Considering the signal conditions under which these frequencies fall in the audio band leads to cumbersome calculations. A more practical approach is to simplify the problem by noticing that as long as the signal is limited to audio frequencies, error signals caused by jitter frequencies above 2 F_A will be outside of the audio range. Hence, only those frequency components of the jitter below 2 F_A need to be considered. This simplification provides an upper limit to the magnitude of the error signal:

$$u_{RMS} \lesssim \frac{1}{T} \, p_{RMS,[0,2F_A]} \, x_{RMS} \qquad \text{with } x_{RMS} = [\, v((k-1)T) - v(kT) \,]_{RMS}$$

if v(kT) is a sine wave, $v(kT) = A \cos(\omega t)$, $x_{RMS} = 2 \sin \frac{\omega T}{2} \, v_{RMS}$, and

$$u_{RMS} \lesssim \frac{2}{T} \, p_{RMS,[0,2F_A]} \sin \frac{\omega T}{2} \, v_{RMS}$$

As expected, the magnitude of the error signal is proportional to the signal amplitude and increases with its frequency. The worst case corresponds to a full scale signal at 20 kHz:

$$u_{RMS} \lesssim \frac{2}{T} \, p_{RMS,[0,2F_A]} \sin(\pi F_A T)$$ relative to full scale. With oversampling filters, $F_A T \ll 1$,

and $$u_{RMS} \lesssim 2\pi F_A \, p_{RMS,[0,2F_A]}$$

Considering two oversampling systems, one operating at 4 x and one operating at 8 x, and assuming the 4 x clock

of the 4 x system to have the same jitter in the [0, 2 F_A] band as the 8 x clock of the 8 x system, the error signals introduced in these two systems by their respective jitters have approximately the same magnitude. However, 4 x and 8 x clocks are generally derived from a 256 x (or 384 x) clock by division. For a given quality of the 256 x clock, and assuming the dividers to be jitter free, the 4 x clock is more jittery than the 8 x clock in the [0, 2 F_A] frequency band, and the 8 x clock itself is more jittery than the 256 x original clock. This shows the importance of measuring the jitter on the actual oversampling clock, rather than on the 256 x clock.

The last formula can be used to calculate the signal degradation caused by a 100 ps RMS random jitter on the oversampling clock. For a full scale signal at 20 kHz, the additional noise is -98 dB.

4.2. CORRELATED JITTER IN DIGITAL-TO-ANALOG CONVERTERS

Let a digital-to-analog converter convert data at a rate mF_S. As in § 4.1., F_S represents the sampling frequency (48 kHz for instance), and m is the oversampling multiplier. The converter is characterized by a propagation delay D from its clock input to its output (this applies to converters both with and without deglitchers). Ideally, D is independent of the output signal. In practice, however, the delay varies with the output level. This variation in delay is called correlated jitter.

While uncorrelated jitter usually produces noise, correlated jitter produces harmonic distortion. A simple example in which the delay is a linear function of the output voltage illustrates this fact. Let the delay D(kT) be equal to $D_0 + \mu\, v(kT)$. The jitter is $\mu\, v(kT)$ and its spectrum follows the signal spectrum. Assuming the signal to be a sine wave of frequency F, the jitter is also a sine wave of frequency F, and the error signal caused by the jitter is a sine wave of frequency 2 F. Non-linear correlations between converter jitter and signal level or signal slope produce harmonics of higher order.

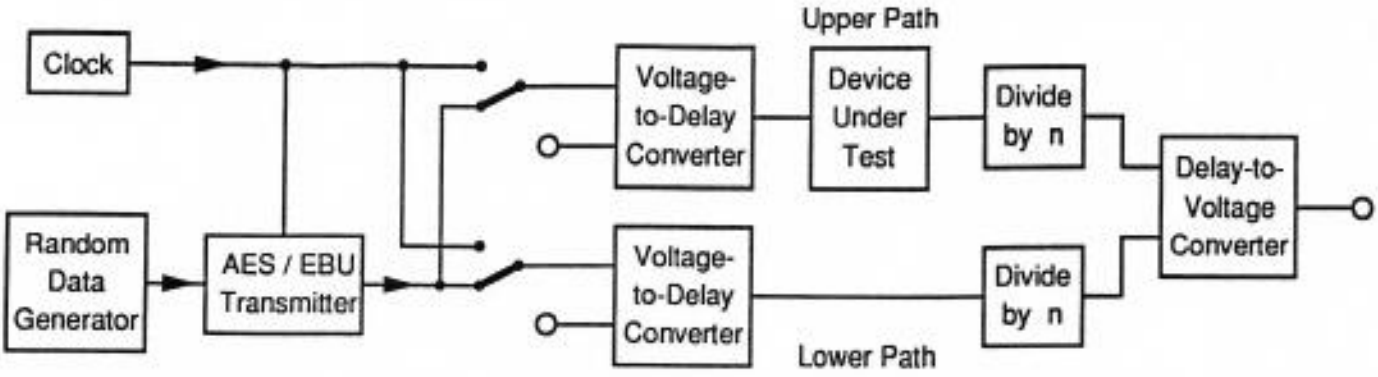
5. MEASUREMENTS

No matter how confident one is of theoretical computations, a measurement instrument is always desirable. Unfortunately, there is no commercially available instrument that will measure jitter with the desired resolution.

There are two basic ways to measure jitter. The arrival time of each edge can be measured with a fixed clock and jitter can be computed from these measurements, or a phase-lock loop circuit can be used to extract the jitter from the signal. The first method is limited in resolution and the prevention of beating between signal and fixed clock is no easy task. The second method relies on a very-low jitter phase-lock loop, and is ill suited for the measurement of low-frequency jitter.

A third method, much simpler, compares a clock signal at the input and at the output of a circuit. Rather than measuring the intrinsic jitter of a signal, it measures how much additional jitter is caused by the circuitry. This yields a very high resolution with a relatively simple tester.

UltraAnalog developed a tester for the evaluation of its products. Its architecture is outlined next page:



The voltage-to-delay converter delays a signal by 30 ns when its control input is grounded. The delay can be varied by applying a voltage on the control input, which has a gain of 1 ns per volt. Any voltage waveform (up to 1 MHz bandwidth), can be applied to the control input, causing jitter of similar waveform on the output of the converter. The noise of the converter itself is about 0.7 ps RMS in the [0, 40 kHz] band when transmitting a 12 MHz clock signal. The delay-to-voltage converter is a delay comparator. The arrival time of each rising edge on the upper input is compared with the arrival time of a corresponding edge on the lower input. The difference is converted to a voltage, stored in a sample-and-hold until the arrival of the next rising edge, and presented on the output. This stage has a gain of 1 volt per ns of differential delay. The noise of the converter itself is about 0.8 ps in the [0, 40 kHz] band when transmitting a 12 MHz clock signal.

This tester can be configured to measure jitter characteristics of AES/EBU receivers. The upper path then consists of an AES/EBU transmitter with a known jitter, a voltage-to-delay converter, the AES/EBU receiver under test, and a low-jitter frequency divider. The lower path consists of a fixed delay, followed by a frequency divider.

The jitter frequency response (attenuation) of the receiver is measured from the voltage-to-delay converter input to the delay-to-voltage converter output. A good receiver will attenuate most of the jitter in the [0, 40 kHz] band. This attenuation also applies to the jitter produced by the AES/EBU transmitter. With the input of the voltage-to-delay converter grounded, the tester output voltage represents the sum of the receiver residual jitter and the attenuated transmitter jitter, which is calculated. The receiver residual jitter is obtained by subtraction. The tester is thus able to measure both the jitter frequency response and the residual jitter of an AES/EBU receiver.

Measurements performed on the Crystal CS8412-CP confirm the manufacturer's published jitter attenuation. The residual jitter of the CS8412-CP, measured on an 8 x oversampling clock derived from the 256 x clock output is found to be between 120 and 200 ps, depending on experimental conditions.

6. CONCLUSION

Close attention must be paid to jitter during the design phase of an audio product. Ideally, all clocks influencing the signal quality should have less that 50 ps of jitter in the [0, 40 kHz range]. AES receivers and other slave clocks, besides having low residual jitter, should have as much jitter attenuation as possible in this frequency band, a first pole at 1 kHz or less being very desirable. Measurements are a necessary design step to ensure that a product will deliver the best possible performance, even under adverse conditions.