

# n-channel JFET

## designed for . . .



- Analog Switches
- Choppers
- Commutators

### Performance Curves NZF

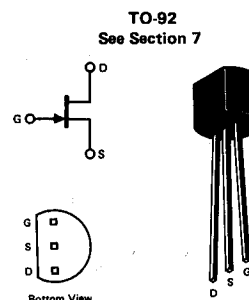
See Section 5

#### BENEFITS

- No Offset or Error Voltages Generated by Closed Switch  
Purely Resistive  
High Isolation Resistance from Driver
- Very Fast Switching  
 $t_{D(on)} + t_r = 6 \text{ ns Typical}$
- Short Sample and Hold Aperture Time  
 $C_{gd(off)} < 2 \text{ pF}$   
 $C_{gs(off)} < 2 \text{ pF}$

#### ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25V  
 Gate Current . . . . . 50 mA  
 Total Device Dissipation at 25°C Ambient  
 (Derate 3.27 mW/°C) . . . . . 360 mW  
 Operating Temperature Range . . . . . -55 to 135°C  
 Storage Temperature Range . . . . . -55 to 150°C  
 Lead Temperature Range  
 (1/16" from case for 10 seconds) . . . . . 300°C



#### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic				J114			Unit	Test Conditions		
				Min	Typ	Max				
1	S T A T I C	IGSS	Gate Reverse Current (Note 1)			-1	nA	VDS = 0, VGS = -15 V		
2		VGS(off)	Gate-Source Cutoff Voltage	-3		-10	V	VDS = 5 V, ID = 1 μA		
3		BVGS	Gate-Source Breakdown Voltage	-25				VDS = 0, IG = -1 μA		
4		IDSS	Saturation Drain Current (Note 2)	15				mA	VDS = 15 V, VGS = 0	
5		ID(off)	Drain Cutoff Current (Note 1)			1	nA	VDS = 5 V, VGS = -10 V		
6		rDS(on)	Drain-Source ON Resistance			150	Ω	VDS ≤ 0.1 V, VGS = 0		
7	D Y N A M I C	Cdg(off)	Drain-Gate OFF Capacitance			2	pF	VDS = 0, VGS = -10 V	f = 1 MHz	
8		Csg(off)	Source-Gate OFF Capacitance			2				
9		Cdg(on) + Csg(on)	Drain-Gate Plus Source-Gate ON Capacitance			8		VDS = VGS = 0		
10		td(on)	Turn On Delay Time		3					
11	tr	Rise Time		3		ns	Switching Time Test Conditions VDD = 10 V, VGS(off) = -12 V RL = 1 KΩ, VGS(on) = 0			
12	td(off)	Turn Off Delay Time		12						
13	tf	Fall Time		8						

#### NOTES:

1. Approximately doubles for every 10°C increase in  $T_A$ .
2. Pulse test duration = 300  $\mu\text{s}$ ; duty cycle  $\leq 3\%$ .

NZF