




Description

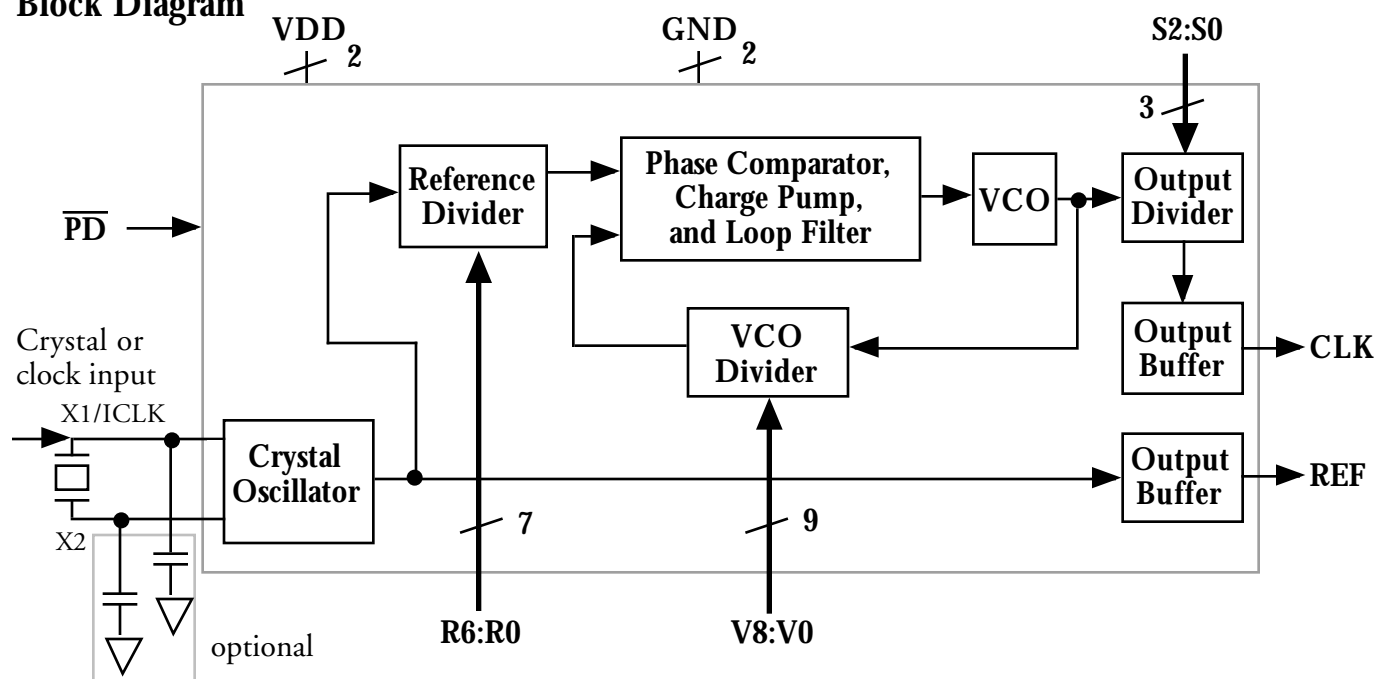
The ICS525 OSCaR™ is the most flexible way to generate a high quality, high accuracy, high frequency clock output from an inexpensive crystal or clock input. The name OSCaR stands for OSCillator Replacement, as it is designed to replace crystal oscillators in almost any electronic system. The user can easily configure the device to produce nearly any output frequency from any input frequency by grounding or floating the select pins. NEITHER MICROCONTROLLER NOR SOFTWARE NOR DEVICE PROGRAMMER ARE NEEDED TO SET THE FREQUENCY. Using Phase-Locked-Loop (PLL) techniques, the device accepts a standard fundamental mode, inexpensive crystal to produce output clocks up to 160 MHz. It can also produce a highly accurate output clock from a given input clock, keeping them frequency locked together.

For simple multipliers to produce common frequencies, refer to the LOCO family of parts, which are smaller and more cost effective.

Features

- Packaged as 28 pin SSOP (150 mil body) 
- Highly accurate frequency generation
- User determines the output frequency by setting all internal dividers
- Eliminates need for custom oscillators
- No software needed
- Pull-ups on all select inputs
- Input crystal frequency of 5 - 27 MHz
- Input clock frequency of 2 - 50 MHz
- Output clock frequencies up to 160 MHz
- Very low jitter
- Duty cycle of 45/55 up to 160 MHz
- Operating voltages of 3.0 to 5.5V
- 25mA drive capability at TTL levels
- Ideal for oscillator replacement
- Industrial temperature version available
- Advanced, low power CMOS process

Block Diagram





MICROCLOCK

ICS525 OSCaR™ User Configurable Clock

Pin Assignment

R5	1	28	R4
R6	2	27	R3
S0	3	26	R2
S1	4	25	R1
S2	5	24	R0
VDD	6	23	VDD
X1/ICLK	7	22	REF
X2	8	21	CLK
GND	9	20	GND
V0	10	19	$\overline{\text{PD}}$
V1	11	18	V8
V2	12	17	V7
V3	13	16	V6
V4	14	15	V5

Output Divider and Maximum Output Frequency Table

S2	S1	S0	CLK	Max. Output Frequency (MHz)			
pin 5	pin 4	pin 3	Output Divider	VDD = 5V		VDD = 3.3V	
				0-70	-40-+85	0-70	-40-+85
0	0	0	10	26	23	18	16
0	0	1	2	160	140	100	90
0	1	0	8	40	36	25	22
0	1	1	4	80	72	50	45
1	0	0	5	50	45	34	30
1	0	1	7	40	36	26	23
1	1	0	9	33.3	30	20	18
1	1	1	6	53	47	27	24

Pin Description

Pin #	Name	Type	Description
1, 2, 24-28	R5, R6, R0-R4	I(PU)	Reference divider word input pins determined by user. Forms a binary number from 0 to 127.
3, 4, 5	S0, S1, S2	I(PU)	Select pins for output divider determined by user. See table above.
6, 23	VDD	P	Connect to VDD.
7	X1/ICLK	X1	Crystal connection. Connect to a parallel resonant crystal, or input clock.
8	X2	X2	Crystal connection. Connect to a crystal, or leave unconnected for clock.
9, 20	GND	P	Connect to ground.
10-18	V0-V8	I(PU)	VCO divider word input pins determined by user. Forms a binary number from 0 to 511.
19	$\overline{\text{PD}}$	I(PU)	Power Down. Active low. Turns off entire chip when low. Clock outputs stop low.
21	CLK	O	Output Clock determined by status of R0-R6, V0-V8, S0-S2 and input frequency.
22	REF	O	Reference output. Buffered crystal oscillator (or clock) output.

Key: I(PU) = Input with internal pull-up resistor; X1, X2 = Crystal connections; O = Output;
P = Power supply connection



Determining (setting) the output frequency

The user has full control in setting the desired output frequency over the range shown in the table on page 2. To replace a standard oscillator, a user should connect the divider select input pins directly to ground (or VDD, although this is not required because of internal pull-ups) during Printed Circuit Board layout, so that the ICS525 automatically produces the correct clock when all components are soldered. It is also possible to connect the inputs to parallel I/O ports to switch frequencies. Contact MicroClock/ICS for tips when using this mode.

The output of the ICS525 can be determined by the following simple equation:

$$\text{CLK frequency} = \text{Input frequency} \cdot 2 \cdot \frac{(\text{VDW}+8)}{(\text{RDW}+2)(\text{OD})}$$

Where Reference Divider Word (RDW) = 1 to 127 (0 is not permitted)
 VCO Divider Word (VDW) = 4 to 511 (0, 1, 2, 3 are not permitted)
 Output Divider (OD) = values on page 2

Also, the following operating ranges should be observed:

$$10 \text{ MHz} < \text{Input frequency} \cdot 2 \cdot \frac{(\text{VDW}+8)}{(\text{RDW}+2)} < \begin{matrix} 320 \text{ MHz at } 5.0\text{V} \text{ or} \\ 200 \text{ MHz at } 3.3\text{V} \end{matrix} \quad \left[\begin{matrix} \text{See Table on Page 2} \\ \text{for full details of} \\ \text{maximum output.} \end{matrix} \right]$$

$$200 \text{ kHz} < \frac{\text{Input Frequency}}{(\text{RDW}+2)}$$

The dividers are expressed as integers, so that if a 66.66 MHz output is desired from a 14.31818 input, the Reference Divider Word (RDW) should be 59, and the VCO Divider Word (VDW) should be 276, with an Output divider (OD) of 2. In this example, R6:R0 is 0111011, V8:V0 is 100010100, and S2:S0 is 001. Since all of these inputs have pull-up resistors, it is only necessary to ground the zero pins, namely V7, V6, V5, V3, V1, V0, R6, R2, S2, and S1.

To determine the best combination of VCO, reference, and output divider, use the ICS525 Calculator on our Web site: <http://www.microclock.com>. This online form is easy to use and quickly shows you up to three options for these settings.

You may also fax this page to MicroClock/ICS at 408 295 9818(fax), or send an e-mail to sales@microclock.com. Be sure to indicate the following:

Your Name _____ Company Name _____ Telephone _____

Respond by e-mail (list your e-mail address) _____ or fax number _____

Desired input crystal/clock (in MHz) _____ Desired output frequency _____

VDD = 3.3V or 5V _____ Duty Cycle: 40-60% _____ or 45-55% required _____



MICROCLOCK

OSCaR™ User Configurable Clock

ICS525

Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (stresses beyond these can permanently damage the device)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+0.5	V
Clock Output	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature	ICS525-01R	0		70	C
	ICS525-01RI	-40		85	C
Soldering Temperature	Max of 10 seconds			260	C
Storage Temperature		-65		150	C
DC CHARACTERISTICS (VDD = 5.0V unless otherwise noted)					
Operating Voltage, VDD		3		5.5	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Input High Voltage, VIH, X1/ICLK only	ICLK (Pin 7)	(VDD/2)+1	VDD/2		V
Input Low Voltage, VIL, X1/ICLK only	ICLK (Pin 7)		VDD/2	(VDD/2)-1	V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
IDD Operating Supply Current, 15 MHz crystal	No Load, 60MHz out		15		mA
IDD Operating Supply Current, 15 MHz crystal	60MHz out, VDD=3.3V		8		mA
IDD Operating Supply Current, Power Down	$\overline{PD}=0$		20		μ A
IDD Operating Supply Current, Power Down	$\overline{PD}=0$, VDD=3.3V		7		μ A
Short Circuit Current	CLK and REF outputs		± 70		mA
On-Chip Pull-up Resistor	V, R, S select, \overline{PD} pins		270		k
Input Capacitance	V, R, S select, \overline{PD} pins		4		pF
AC CHARACTERISTICS (VDD = 5.0V unless otherwise noted)					
Input Frequency, crystal input		5		27	MHz
Input Frequency, clock input		2		50	MHz
Output Frequency with OD=2, VDD = 4.5 to 5.5V	0 C to 70 C	1		160	MHz
	-40 C to +85 C	1		140	MHz
Output Frequency with OD=2, VDD = 3.0 to 3.6V	0 C to 70 C	1		100	MHz
	-40 C to +85 C	1		90	MHz
Output Clock Rise Time	0.8 to 2.0V		1		ns
Output Clock Fall Time	2.0 to 0.8V		1		ns
Output Clock Duty Cycle, even output dividers	at VDD/2	45	49 to 51	55	%
Output Clock Duty Cycle, odd output dividers	at VDD/2	40		60	%
Power Down Time, \overline{PD} low to clocks stopped low				50	ns
Power Up Time, \overline{PD} high to clocks stable				10	ms
Absolute Clock Period Jitter	Deviation from mean		± 90		ps
One Sigma Clock Period Jitter			40		ps

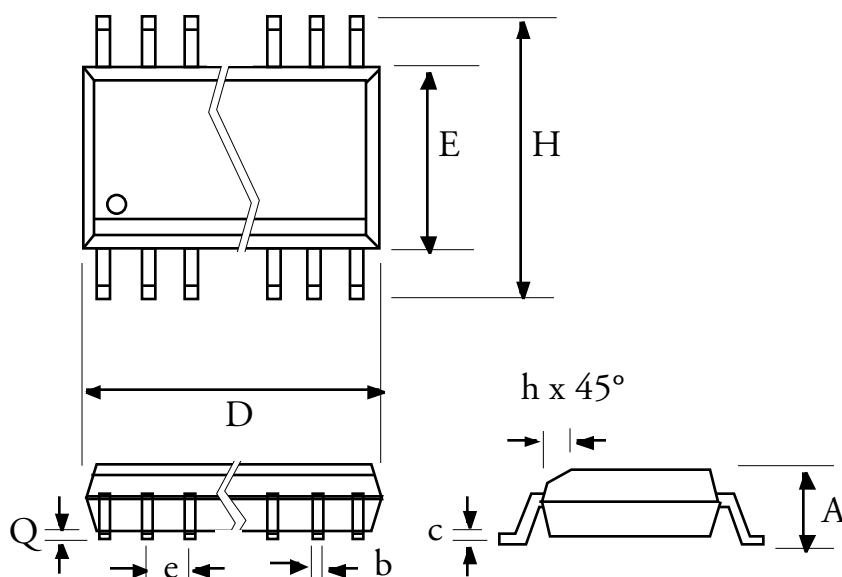


External Components / Crystal Selection

The ICS525-01 requires two 0.01 μ F decoupling capacitors to be connected between VDD and GND, one on each side of the chip. They must be connected close to the ICS525-01 to minimize lead inductance. No external power supply filtering is required for this device. A 33 Ω terminating resistor can be used next to the CLK and REF pins. The total on-chip capacitance for a crystal is approximately 16 pF, so a parallel resonant, fundamental mode crystal with this value of load (correlation) capacitance should be used. For crystals with a specified load capacitance greater than 16 pF, crystal capacitors may be connected from each of the pins X1 and X2 to Ground as shown in the Block Diagram on page 1. The value (in pF) of these crystal caps should be = $(C_L - 16) * 2$, where C_L is the crystal load capacitance in pF. These external capacitors are only required for applications where the exact frequency is critical. For a clock input, connect to X1 and leave X2 unconnected (no capacitors on either).

Package Outline and Package Dimensions

28 pin SSOP



	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.061	0.068	1.55	1.73
b	0.008	0.012	0.203	0.305
c	0.007	0.010	0.191	0.254
D	0.385	0.400	9.779	10.160
E	0.150	0.160	3.810	4.064
H	0.230	0.245	5.842	6.223
e	.025 BSC		0.64 BSC	
h		0.016		0.406
Q	0.004	0.01	0.102	0.254

Ordering Information

Part/Order Number	Marking	Package	Temperature
ICS525-01R	525-01R	28 pin narrow SSOP	0 to 70 C
ICS525-01RT	525-01R	28 pin SSOP on tape and reel	0 to 70 C
ICS525-01RI	525-01RI	28 pin narrow SSOP	-40 to +85 C
ICS525-01RIT	525-01RI	28 pin SSOP on tape and reel	-40 to +85 C

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