I2S FIFO Firmware V3.80 Upgrading

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New features of firmware V3.80

Optional default 512*Fs MCLK frequency setting for Single XO Clock Board

Optional left justified FIFO output format

Optional left justified, 16 bit right justified, 24 bit right justified FIFO input format

Additional I2S input port support for S/PDIF Interface Board

512*Fs default MCLK frequency setting for Single XO Clock Board

This feature will benefit the Single XO Clock Board user by making use of higher frequency XO (for example, use 22.5792 MHz XO for 44.1 KHz), or same XO frequency for two Fs (for example, use 22.5792 MHz XO for both 44.1 KHz and 88.2 KHz). This upgrade does not apply or affect Dual XO Clock Board.

Jumper settings	Single XO Clock Board XO frequency required	
TP48 left open	MCLK = 256 * Fs	Factory default
TP48 short to GND	MCLK = 512 * Fs	

Cross reference table of XO frequency selecting with Single XO Clock Board

Fs	44.1 KHz	48 KHz	88.2 KHz	96 KHz	176.4 KHz	192 KHz
Set MCLK=256*Fs	11.2896M	12.2880	22.5792M	24.5760	45.1584M	49.1520M
Set MCLK=512*Fs	22.5792M	24.5760	45.1584M	49.1520	-	-

FIFO output format settings

Jumper settings	Output format	
TP43 left open	I2S (word width 32 bit)	Factory default
TP43 short to GND	Left justified (word width 32 bit)	

FIFO input format settings

TP41	TP42	Input format	
Left open	Left open	I2S (16bit-32bit)	Factory default
Short to GND	Left open	Left justified (16bit-32bit)	
Left open	Short to GND	right justified 6 bit	
Short to GND	Short to GND	right justified 24 bit	

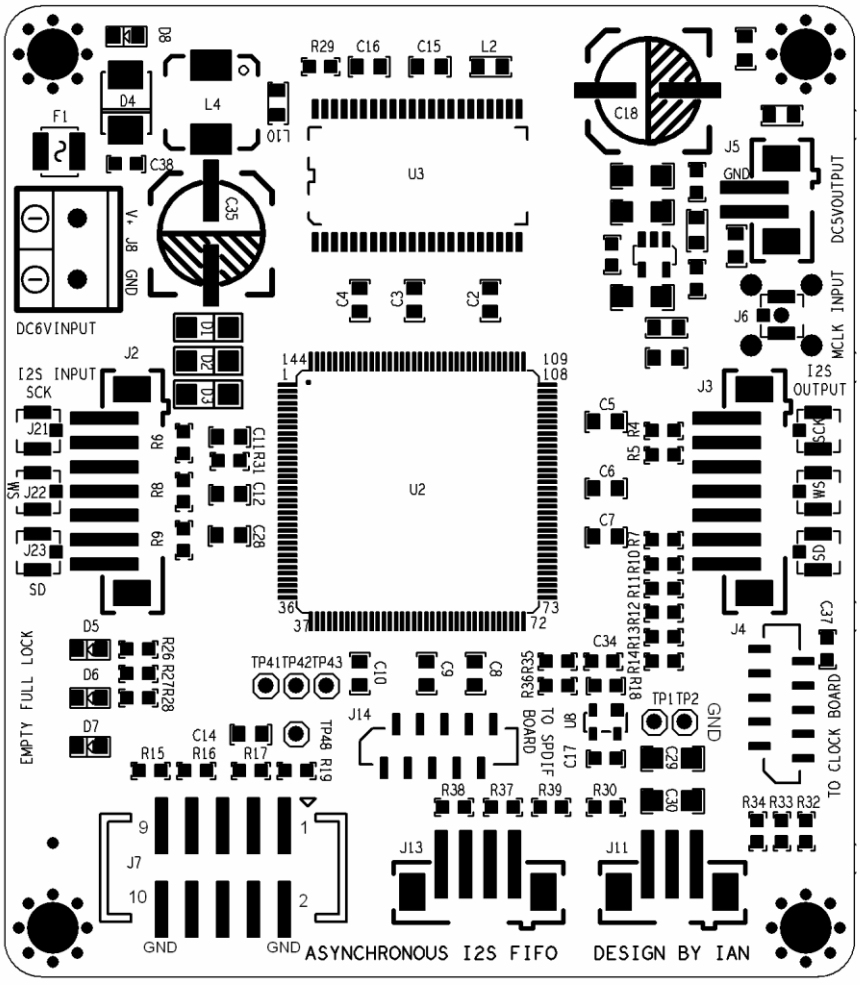
Additional I2S input port support for S/PDIF Interface Board

With S/PDIF Interface Board connected to the FIFO Board, the additional I2S input port will be supported and included in the input scan loop automatically by firmware V3.80 or higher. The sources selecting loop will become OPT -> COX -> TTL -> I2S -> Loop back when press the button on the S/PDIF Interface Board. Please see the corresponding document of S/PDIF Interface Board for details.

Jumper and terminal locations

Please see the picture below for jumper TP41, TP42, TP43 and TP48 locations.

Please note that the GND terminals are located at pin J7.2, J7.10 and TP2



Application notes and tips

1. Jumpers and connectors will be included in the KIT. Please do not assemble them if you don't need those new features. Keeping the original factory default settings is recommended.

2. Connecting the jumper cables together if you don't have enough GND terminals.

3. Jumper cables may need to be cut shorter and re-connected to fit your application.

4. Power supply has to be turned off during setting the jumpers.

5. Please check the barcode tag on the back of the FIFO board PCB for the firmware versions.