High Power Adjustable Load

with power limiter

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An adjustable load resistance is indispensable for the realistic testing of power output stages. This circuit provides an electronic alternative to the use of inconvenient high-wattage resistors.

Technical specifications

Input voltage:	0 to +100 V_{DC}
Sink current:	0 to 20 A
Load resistance:	<1 Ω to >100 kΩ
Maximum power dissipation:	approximately 100 W
Linearity error:	<0.5 %

The circuit described here has two modes of operation. It can function as an adjustable current sink or as a variable load resistance. At a voltage of between 0 V and a maximum 100 V the sink current can be set in the range 0 A to 20 A. As a load resistance it can be set to values from less than 1 Ω to more than 100 kΩ. The maximum power dissipation is in the region of 100 W. The circuit is designed for operation with DC voltages, but with the addition of a rectifier can also be used with (low frequency) AC voltages. A carefully constructed and calibrated unit can deliver a linearity of better than 0.5 %.

Current Sink and Load Resistance

Let us first consider the circuit as a current sink (S2 in position 'CC': constant current) initially ignoring the part of the circuit consisting of the three op-amps IC1.B, IC1.C and IC1.D and the surrounding components.

The load circuit consists of a power FET and resistor R2. An electrolytic capacitor is connected in parallel with these, smoothing the voltage across the FET and R2 and suppressing spikes. The FET is controlled by IC1.A. The op-amp attempts to keep the voltage at its inverting input (that is, the voltage across R2) the same as that on its non-inverting input. The latter is in turn equal to the voltage on the wiper of 10-turn potentiometer P1. We have therefore achieved what we sought to achieve: the current drawn is proportional to the wiper setting of P1. This means, of course, that the wiper voltage of the potentiometer must be kept constant, and this is guaranteed by the 2.5 V voltage reference D7. At the upper limit of the potentiometer's travel we have a voltage of 0.779 V (because of R3), assuming that S1 is open.

Only the first five turns of the ten-turn potentiometer can be used before the power limiter comes into effect. If the current sink is to be used within its power limits, a smaller range of voltages across R2 is more useful: this is the function of R12 and trimmer P2. When S1 is closed these are connected in parallel with P1 and are adjusted so that the voltage is reduced by a factor of ten. This allows a current setting in the range 0 A to more than 5 A.

If S2 is switched to position 'CR' (constant resistance), a different voltage is applied across P1. The source is no longer provided by the voltage reference but by the input voltage. The remainder of the circuit works as before, meaning that the input current is proportional to the input voltage, and the constant of proportionality is equal to the constant resistance. With R4 being 475 kΩ load resistances from infinity to 1 Ω (at the extreme settings of P1) can be achieved.

Power Limiter

The remaining three op-amps in the LM348 form a power limiter to ensure that the power dissipation of the circuit remains under control. An analogue multiplier is not used in this circuit. R10 and R11 form a voltage divider across the input voltage, which operates linearly as long as diode D2 does not conduct. This does not happen abruptly, but rather follows the characteristic curve of the diode, providing a gradual transition as the input voltage rises. IC1.C buffers this voltage and drives

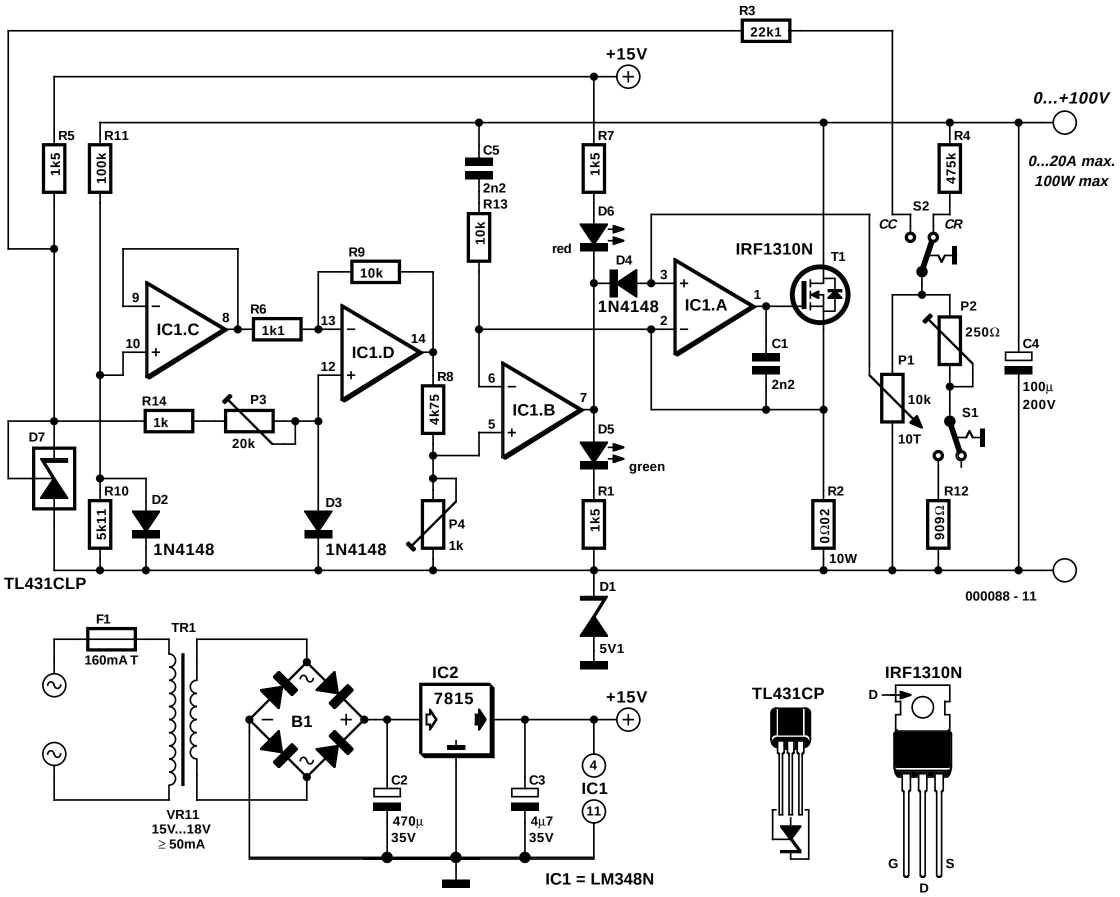

Figure 1. An op-amp, a resistor and a FET form the basis of this item of test equipment.

inverter IC1.D, which inverts the characteristic curve of the diode and amplifies it with a gain of ten. The output voltage of the op-amp is raised by an amount equal to the diode forward voltage via D3.

The operating point of D3 is determined by the reference voltage, R10 and the setting of trimmer P3. Finally, comparator IC1.B compares the output voltage of the inverter with the voltage across R2 and, if the power limit is exceeded, pulls down the control voltage to op-amp IC1.A, turns off the green 'OK' LED and lights the red 'warning' LED.

Note that this is only a crude protection circuit for limiting the power above about 100 W. It is highly dependent on device-to-device variations among diodes and on temperature, but is entirely adequate for protecting against excessive current draw from, for example, a 12 V car battery.

The circuit as a whole is powered from a mains power supply, which as usual consists of a mains transformer (15 V to 18 V, at least 50 mA), a bridge rectifier and a 15 V fixed voltage regulator.

C2 smoothes the rectified DC voltage and C3 suppresses transients. Since the op-amps are operating near to the lower input voltage, a negative supply is required for them (unless rail-to-rail types are resorted to). To this end Zener diode D1 provides a negative supply voltage about 5 V below the lower input voltage.

Construction and Calibration

Since we have not shown a printed circuit board layout for this circuit, a few words on construction are in order. The circuit presents no enormous technical difficulties, and simple prototyping board will suffice for construction, but a suitably heavy-duty enclosure must be found. The FET must be able to dissipate up to about 85 W under peak conditions, and the heat must be carried away using a large heat sink. The data sheet for the FET indicates that a heatsink rated at 0.9 K/W or better is required. Alternatively, the FET can be fitted with a modern CPU fan. The circuit is intended for hobby use or for short laboratory tests, and not for continuous use (for example 24 hour soak tests). If additional thermal protection for the transistor is desired, a thermal relay (closing at 105 °C) can be fitted. The relay is glued to the transistor using two-part adhesive, and wired so as to short pin 3 of IC1.A to the lower input potential.

If you do not wish to fit a fan, but nevertheless want to operate either at high loads or continuously, then you can connect up to five FETs in parallel (for example type BUZ344). The circuit also works well with 150 W to 200 W power Darlingtons such as the MJ11016 in a TO3 package, but not in a parallel arrangement and only with input voltages above 1 V.

R2 also plays its part in dissipating power. Either a 15 W power resistor should be fitted, a few millimetres above the surface of the circuit board, or a 10 W power resistor in a metal housing with heatsink can be used.

The FET, the power resistor R2 and electrolytic C4 should be placed next to one another centrally on the rear side of the (horizontally-mounted) circuit board, with the two high-current terminals (a suitable type is available from AMP) on either side. The components should be connected with thick wire, taking care not to overheat the components when soldering.

The control electronics should be placed immediately next to the FET, and in particular the connection between the output of the control op-amp IC1.A and the gate of the FET should be short.

Since the electronics are fitted at the rear of the enclosure, the components fitted to the front panel (S1, S2, P1, the LEDs and the two banana sockets) must be wired to the circuit board. For the input we have already suggested AMP connectors, while for the remaining — low power — connections ordinary signal wire will do.

The power supply can be fitted in a spare corner of the circuit board. The mains enters via a switched and fused input socket, which avoids having the mains switch on the front panel. LED D5 serves as a power indicator.

In the interests of safety, the 'thin' wiring should be kept well separated from the power supply and from the thick input wiring.

Check over the circuit once more, fit it into the enclosure and check the wiring and that the heatsink is isolated from the FET (!), and switch on at the mains. Assuming that no smoke appears, and that the supply and reference voltages are correct, the unit can be switched off again and the LM348 fitted in its socket. The control circuit can now be calibrated.

Turn the unit on again and apply a voltage of 10 V to the input. The voltage at pin 13 of the IC should be the same as that on pin 12 (P3). At the output of IC1.D a voltage of 0.95 V should be measured, and we want the current through the FET to be limited to about 10 A. Adjust P4 to set the voltage on pin 5 to 200 mV. This corresponds to a current of 10 A at 10 V (or 100 W). You will find that a little patience is required in adjusting P3 and P4. The adjustment of P2 has been described above. The calibration is now done: fit the lid to the enclosure and your unit is complete.

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