

# **I2S FIFO KIT with attached frame and Single XO Clock Board user guide**

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## **Principle description**

The digital audio stream consists of two parts: data and clock. Usually we don't have any problem with data. But the clock is not perfect (there is no ideal clock in the real world); it comes with jitter (or phase noise). Jitter is the main reason why different digital audio sources sound different even when they play the same audio stream.

An asynchronous I2S FIFO is a kind of logic device which can buffer the digital audio stream, allowing the audio data to pass through but isolating the original clock and replacing it with a new one (secondary clock). If the new clock has less phase noise than the old one, the digital audio stream after the FIFO will have less jitter and that will make the DAC or other digital audio device playing the stream sound better. Moreover, the sound quality of the playback will be independent from the digital audio source. So, together with clock technology, the I2S FIFO is firmly believed to be one of the most effective solutions to deal with jitter.

## **Introduction**

This I2S FIFO KIT is an open-concept design created especially for audiophiles with the most up to date technology. The basic kit includes the I2S FIFO Board and a Single XO Clock Board together on one piece of PCB.

When used with an upgraded clock or clock board (available separately), the KIT's performance can be improved and the sound quality of the subsequent device can be improved dramatically.

By adding an S/PDIF board (also available separately), a S/PDIF FIFO could be set up. Digital audio sources with S/PDIF output, such as CD transports, digital audio players (like Squeezebox, AppleTV and so on), DATs, and even PC, Mac or Linux software players, can obtain the benefits of the FIFO concept.

The KIT is a very flexible and expandable modularized FIFO solution.

## KIT includings

- An assembled and tested I2S FIFO PCB with attached frame and Single XO Clock Board
- Two 8" single-ended PH 2.0mm 7-pin I2S cables
- One 2" double-ended PH 2.0 mm 7-pin I2S bridge cable (already connected on the board)
- One 6" double-ended U.FL cable for MCLK
- One SMT U.FL receptacle (used only in limited applications for MCLK)
- One 2" 10-pin FPC/FFC cable (already be connected on the board)
- Four ¼" rubber rings to attach the clock board to its frame
- An 11.2896 MHz oscillator comes installed on the Single XO Clock Board for function verification

## I2S FIFO Board features and specifications

- I2S input
  - LVTTTL (3.3V) logic input level with TTL (5V) tolerance
  - 44.1 KHz, 48 KHz, 88.2 KHz, 96 KHz, 176.4 KHz, 192 KHz - 16bit, 24bit or 32bit
  - 7-pin PH 2.0mm connector, or
  - Three 50 ohm U.FL coaxial connectors
- I2S output
  - LVTTTL (3.3V) logic output level
  - 44.1 KHz, 48 KHz, 88.2 KHz, 96 KHz, 176.4 KHz, 192 KHz - 16bit, 24bit or 32bit
  - 7-pin PH 2.0mm connector, and
  - Three 50 ohm U.FL coaxial connectors
- MCLK input
  - LVTTTL (3.3V) logic output level
  - 128\*Fs, 256\*Fs (default) or 512\*Fs
  - Optional 50 ohm U.FL coaxial input connector (not used if using the clock board)

- FIFO Memory

- 4Mb SRAM
- Speed 10ns

- FIFO half full delay time

Fs	44.1KHz	48KHz	88.2KHz	96KHz	176.4KHz	192KHz
Delay (s)	0.74	0.68	0.37	0.34	0.18	0.17

- Future clock board integration

- Can be integrated with attached single XO clock board or upgraded to a higher quality, multi-frequency clock board (such as Dual XO Clock Board) that comes with automatic Fs switching and better performance
- 10-pin FFC/FPC clock board control port
- Universal clock board frame compatible with all dedicated clock boards
- Rubber ring suspensions are provided to improve clock performance by reducing mechanical vibration (you will need to cut the clock board from its frame)
- Upgrading and replacing the clock board is very easy, just remove the old one and hang the new clock board to the frame using the rubber rings (or just stack over the clock frame).

- Future S/PDIF Interface Board integration

- 10-pin FFC/FPC S/PDIF board control port
- S/PDIF FIFO can be set up by expanding with an S/PDIF Interface Board

- LED indicators for power, I2S lock, FIFO status

- DC power supply

- 6V 500mA
- Absolute minimum voltage: 4.5 V - Absolute maximum voltage 6.7 V - On board TVS protecting the FIFO board from damage by over voltage
- On board PTC resettable fuse for over current protection

## Single XO Clock Board features and specifications

- Clock oscillator

- The oscillator socket is compatible with all standard square or rectangular 3.3V DIP XOs with 8- or 14- pin footprints
- Supports 44.1 KHz, 48 KHz, 88.2 KHz, 96 KHz using XOs with different frequencies, MCLK is fixed at  $256 \cdot F_s$ .

$F_s$	44.1KHz	48KHz	88.2KHz	96KHz
XO frequency	11.2896MH	12.2880MH	22.5792MH	24.5760MHz

- An 11.2896 MHz clock oscillator is supplied with the KIT for function verification. The supplied oscillator is a generic XO. To boost the sound quality, a high-performance, low jitter XO clock is required.
- 50 ohm U.FL coaxial connector for MCLK output

- I2S re-clock input

- LVTTTL (3.3V) logic input level – 7-pin PH 2.0mm connector

- I2S re-clock output

- LVTTTL (3.3V) logic output level
- 7-pin PH 2.0mm connector, and
- Three 50 ohm U.FL coaxial connectors
- Max re-clocking frequency: 550 MHz

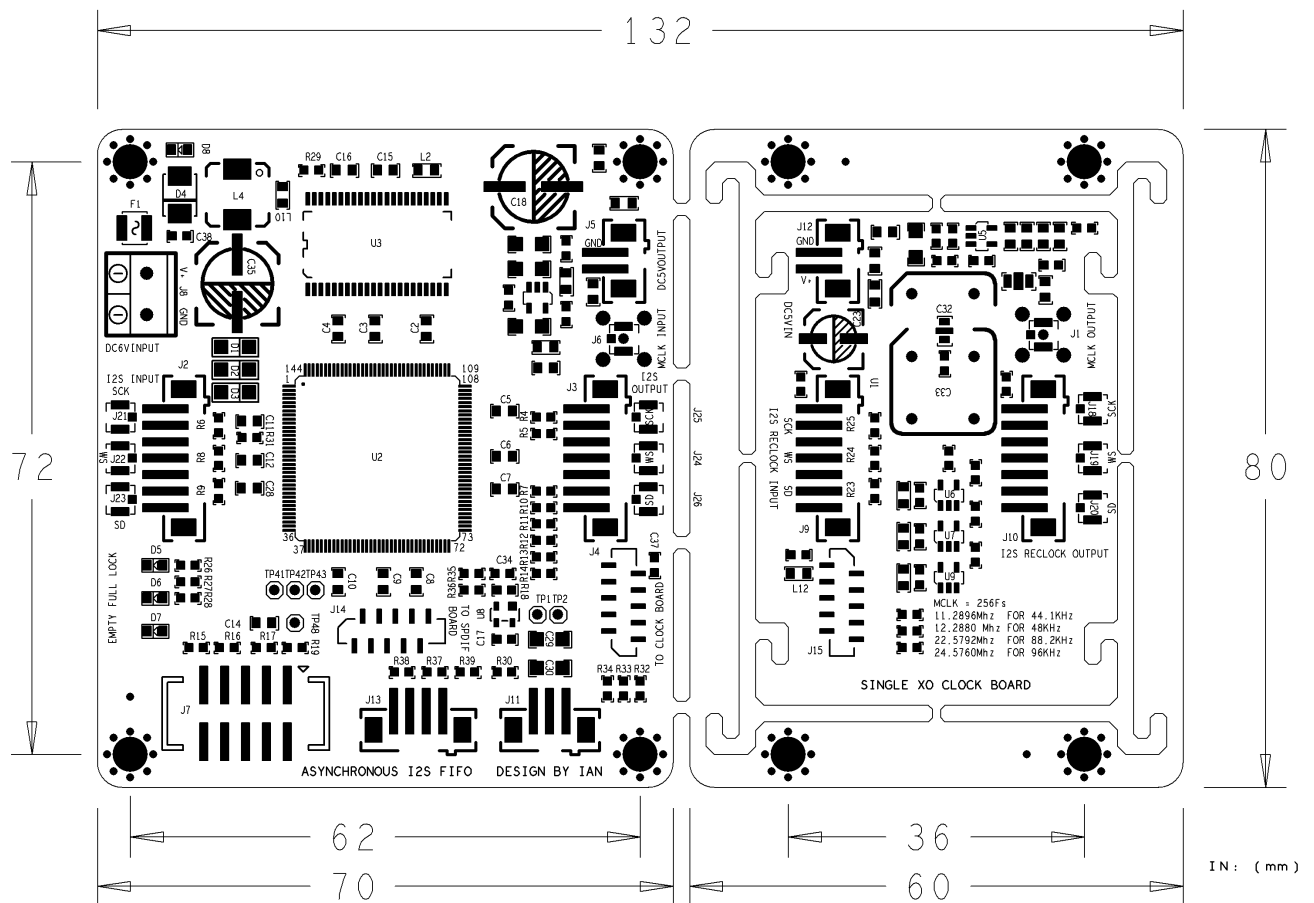
- Power supply

- On-board 9 $\mu$ V RMS low-noise, high-PSRR LDO
- EMI filters equipped to improve the performance

- Upgrading

- Upgrading to a higher grade multi-frequency clock board (such as the Dual XO Clock Board) is required to support full working range of the I2S stream from 44.1 KHz to 196 KHz and to utilize the  $F_s$  automatic switching function.

## Layout and dimensions



## Connectors on the I2S FIFO Board

- Power input: DC6V via a 2-pin 5.0mm terminal block
- I2S input:

J2, a single PH 2.0mm 7-pin connector, configured as:

1	2	3	4	5	6	7
GND	SCK	GND	WS	GND	SD	GND

or, three U.FL coaxial cable connectors, configured as:

J21	J22	J23
SCK	WS	SD

- I2S output (which must be connected to the clock board I2S input port if using the re-clock function):

J3, a PH 2.0mm 7-pin connector, configured as:

1	2	3	4	5	6	7
GND	SCK	GND	WS	GND	SD	GND

or, three U.FL coaxial cable connectors, configured as:

J25	J24	J26
SCK	WS	SD

- Optional MCLK input: J6, U.FL coaxial cable connector (this is not used when using the on-board clock)
- Clock board interface: J4, FPC/FFC 1.0mm 10-pin connector, double-sided contacts
- S/PDIF board interface: J14, FPC/FFC 1.0mm 10-pin connector, double-sided contacts
- Optional control signals output port: J13, PH 2.0mm 4-pin connector (This is not used in most applications. It is used with some DACs, or other devices, that need these signals). The configuration is:

1	2	3	4
SILENCE	128Fs	512Fs	GND

SILENCE	Function
1	To silence the DAC
0	Normal operating

512Fs	128Fs	MCLK VS. output I2S Fs
1	1	256 * Fs
1	0	512 * Fs
0	1	128 * Fs
0	0	Reserve

- Connectors reserved for future applications: J5, J7, and J11 (these should not be changed unless specific instructions direct differently)

## Connectors on the Single XO Clock Board

- MCLK output: J1, U.FL coaxial cable connector
- I2S re-clock input: J9, PH 2.0mm 7-pin connector, configured as:

1	2	3	4	5	6	7
GND	SCK	GND	WS	GND	SD	GND

- I2S re-clock output: J10, PH 2.0mm 7-pin connector, configured as:

1	2	3	4	5	6	7
GND	SCK	GND	WS	GND	SD	GND

and, U.FL coaxial cable connectors, configured as:

J18	J19	J20
SCK	WS	SD

- XO socket: U1
- The socket supports standard DIP 3.3V clock oscillators with 14- or 8- pin footprints
- FIFO board interface: J15, FPC/FFC 1.0mm 10-pin connector, double side contacts
- Connectors reserved for future applications: J12, DC input (these should not be changed unless specific instructions direct differently)

## LED indicators

D8: Power indicator

D5: I2S input lock indicator

Off: I2S input signal is out of the FIFO's operating range (i.e., not a valid I2S stream)

On: I2S input signal is locked

D6: FIFO full indicator

Off: FIFO is not full

On: FIFO is full

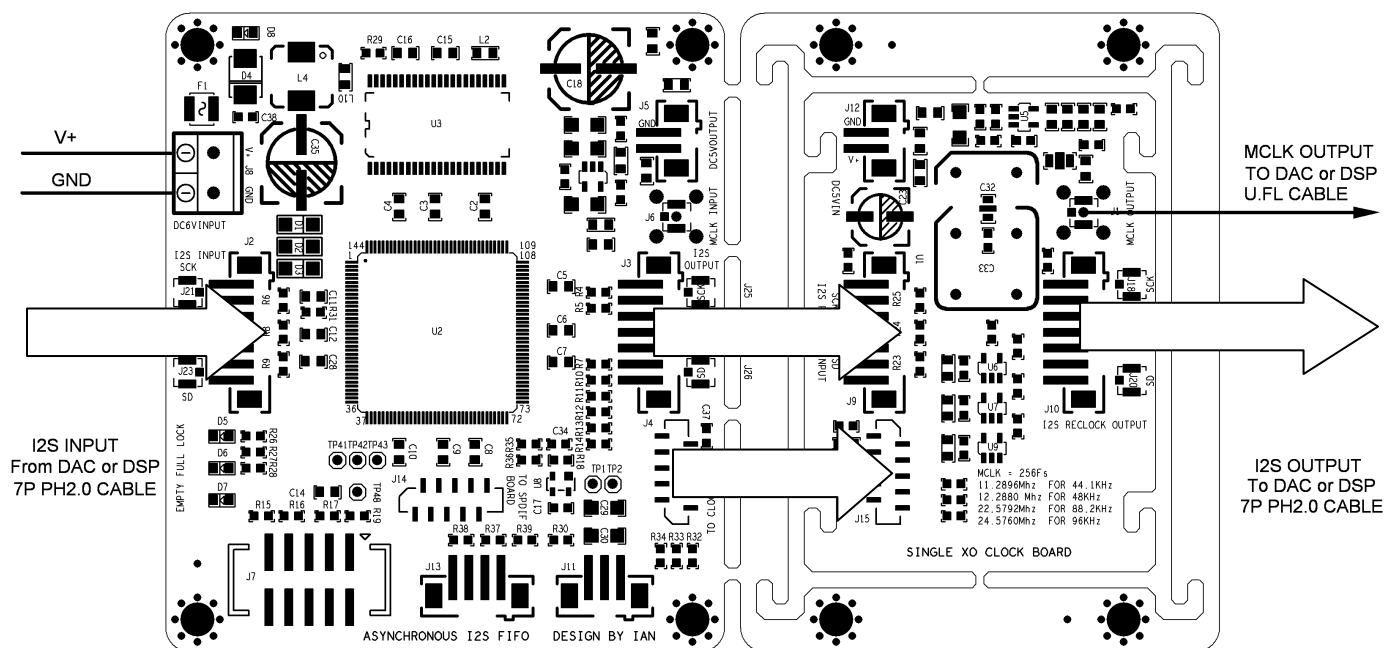
D7: FIFO empty indicator

Off: FIFO is not empty

On: FIFO is empty

## Connecting to a DAC or DSP with PH 2.0mm 7pin cables

This is the most common way to connect the FIFO KIT with a DAC or other digital audio device. This configuration works well in most applications because many DACs and DSPs are just sensitive to jitter from the MCLK.





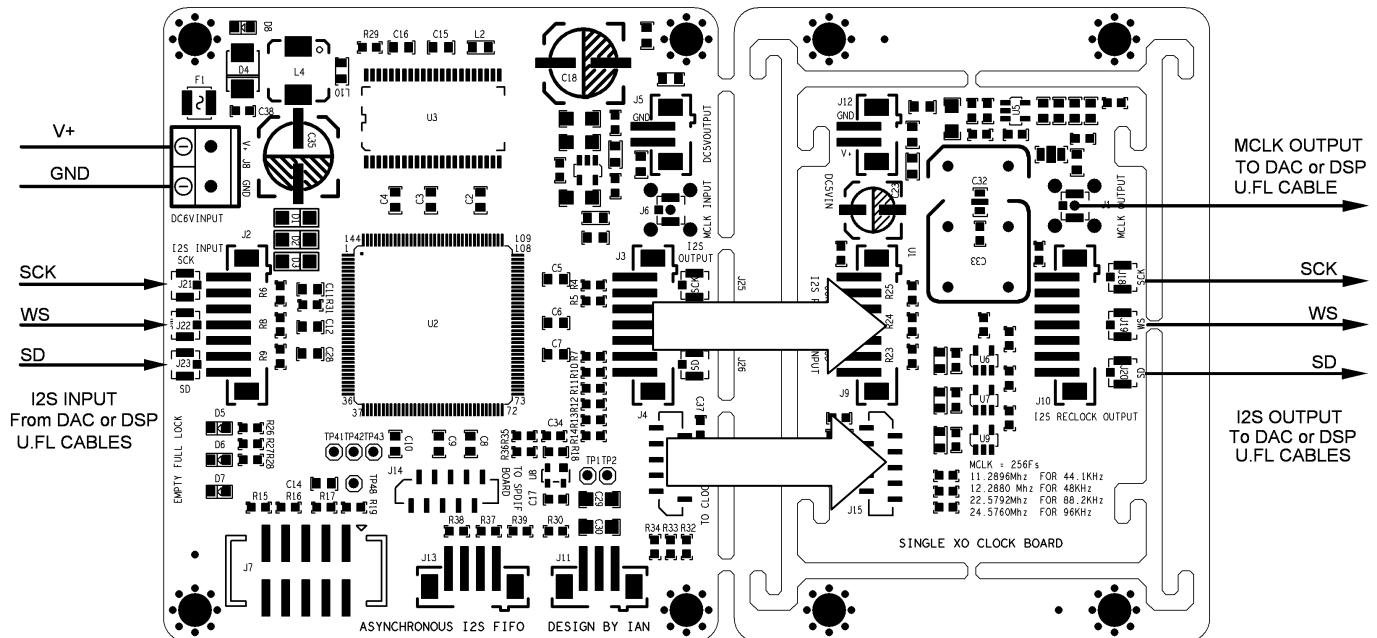
## Connecting to a DAC or DSP with U.FL coaxial cables

Better signal quality can be achieved using coaxial cable. Coaxial cable is highly recommended for all applications, but especially for those NOS DACs which use only the I2S signal.

A U.FL tool is recommended for un-plugging the U.FL cables. Otherwise, both the connector and the head of the cable could be damaged during removal. A tool is available here:

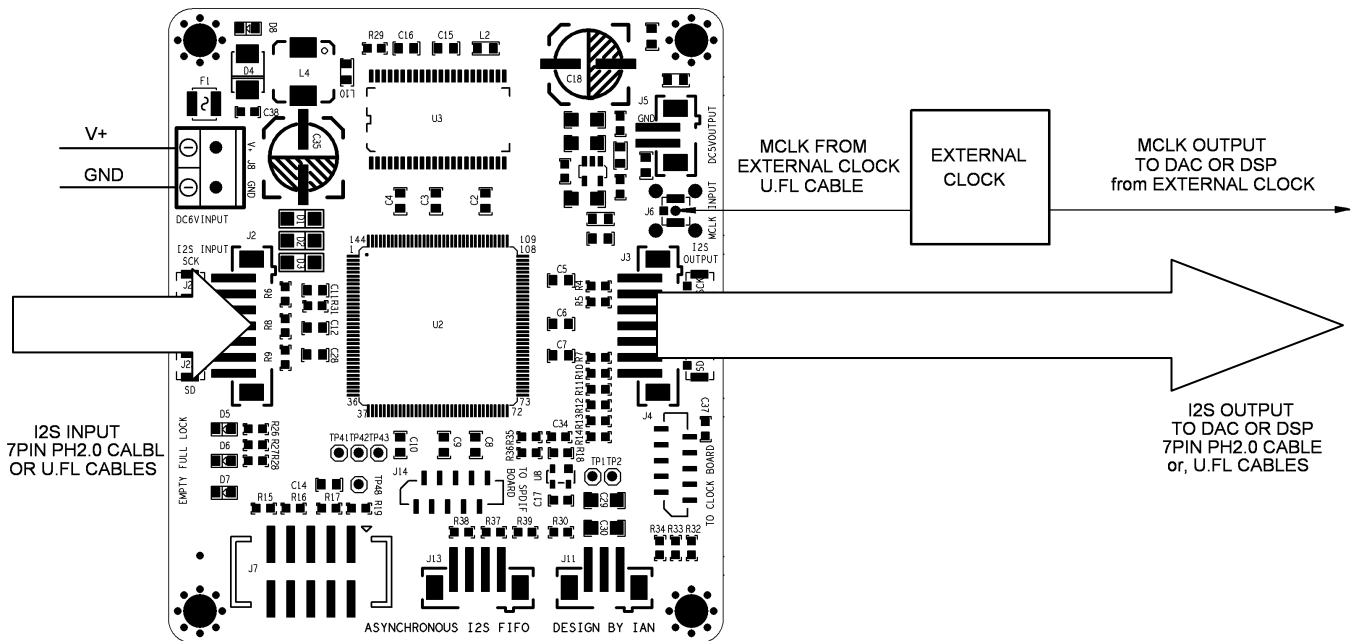
<http://search.digikey.com/us/en/products/U.FL-LP-N-2/H9159-ND/513008> Or, you can make one yourself.

It is also possible to use coaxial cables only for MCLK and the I2S outputs while keeping the I2S input connected by the PH 2.0mm 7-pin cable. This is because the MCLK and I2S signals after FIFO are independent from the input I2S signals.



## Connecting to a DAC or DSP with external clock source

This configuration is not recommended for normal applications.



If this configuration is really needed, it is highly recommended to connect the external clock directly to the XO socket on the clock board. For external clock, the logic level of MCLK input on the I2S FIFO Board must be LVTTTL (3.3V) and the MCLK frequency must be fixed at  $256 \cdot F_s$ .

## Available Upgrades

### Multi-frequency clock board:

Based on an open concept, different kinds of dedicated clock boards can be designed with various clock solutions. By using an upgraded clock board, the Dual XO Clock Board, for example, the performance of the I2S FIFO KIT can be improved.

Compared to the Single XO Clock Board which is included in the basic FIFO KIT, dedicated clock boards usually come with the following advantages:

- Multi-frequency output capability to support the full I2S working range from 44.1 KHz to 196 K
- Automatically switching frequencies according to the input I2S signals
- Fan-out buffer to improve the clock performance by reducing the additive jitter of MCLK drivers and improving isolation between the branches of the clock tree
- Enhanced power supply and EMI filters

Please refer to the user's manual of the corresponding clock board for more details.

### S/PDIF interface board:

A S/PDIF Interface Board could be integrated into the FIFO KIT to include the DIR and DIT function. Please refer to the user's manual of S/PDIF Interface Board for more details

## Application notes and tips

### - Selecting the DC power supply

The phase noise performance of the clock is very sensitive to the clock's power supply. Thus the DC power supply should be chosen with care. Although low-noise, high-PSRR LDOs and EMI filters are included on the board, low noise, high performance DC power is preferred. A low noise shunt regulator is a good choice. Batteries are a good alternative. Both 6V lead batteries (>4AH) and 6.4V LiFeP04 batteries (>2AH) were tested with good results.

(Please note that, while protection circuits are included on the I2S FIFO Board, over-voltage or reverse polarity connection still may risk damaging the board).

### **- Selecting the Oscillator**

Low phase noise clock oscillators are essential to the best sound quality. When selecting an oscillator, the parameters of both the phase noise floor and the close-in phase noise (e.g. at 100 Hz off-set) have to be analyzed carefully to make the right selection. Various high-performance, but expensive, XOs (including SC cut XOs), are preferred. Good results at a reasonable price have been achieved, however, but not limited with the Crystek CCHD-957 series and the Silicon Labs Si570 and Si532 series.

Trying different clock oscillators is an interesting experience. Even clocks with the same jitter level may sound slightly different because of differences in the phase noise characteristics. Some clocks provide more detail; others sound more “musical.” The modular nature of the FIFO board encourages you to try different solutions and choose one according to your personal preference and the style of music.

For some generic clock oscillators, the internal crystal may not be that bad. The problem is usually that generic oscillators do not have a well designed power supply and associated circuit. In many cases, if fed with a high quality, low noise power supply and interfaced with a low jitter output buffer, they will perform better than originally.

### **- Clock jitter and sound quality**

Low jitter clock: stereo imaging is better focused on a fixed point; more detailed, more dynamic, crystal clear; the sound stage is more three-dimensional - everything can be distinguished; dark and deep background. Over-all, the sound is closer to “real.”

High jitter clock: the sound seems to come from a wide area without focus; a mixed up, noisy background; difficult to distinguish different instruments; ear fatigue. Over-all, more “digital” than the real sound.

### **▪ Sampling clock and legacy CDs**

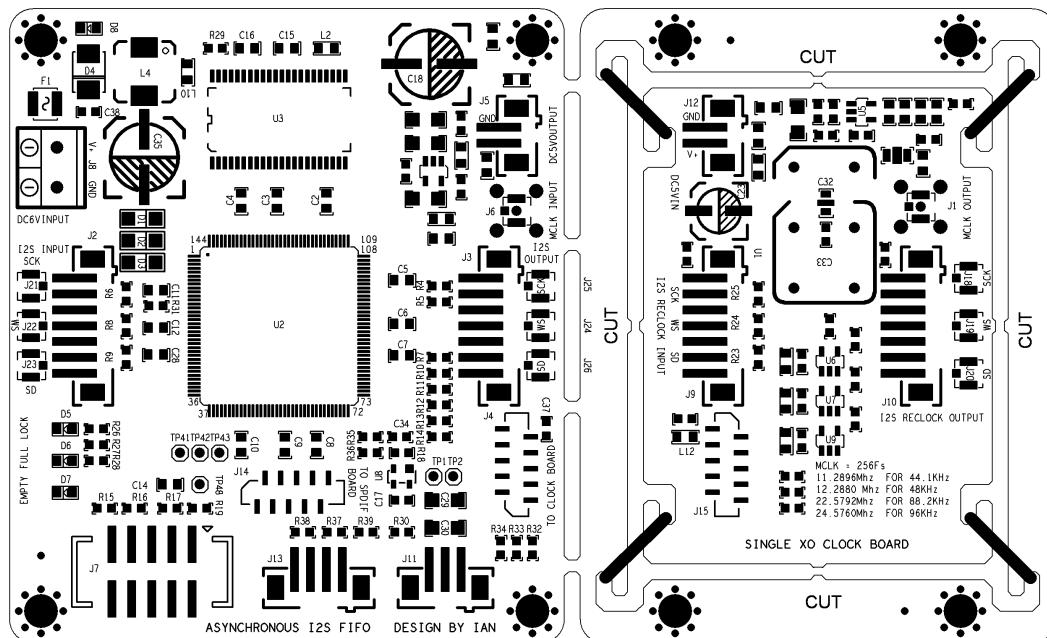
Digital recording technology has improved dramatically since the first redbook CD was introduced decades ago.

Most of the new digital music tracks were recorded with very good sampling clocks. The FIFO concept works very

well with them. However, some older digital music tracks and legacy CDs, for example, things from 1980's, were recorded with poor sampling clocks. For these older tracks and CDs, the sound quality will enjoy limited

### ▪ Hooking up rubber ring suspensions

Hook up the four rubber rings at each corner of the clock board, and then cut off the four connecting bars between the frame by a side cutter. Sand the cutting section with a file if possible.



## Reference

I2S bus specification: [http://www.classic.nxp.com/acrobat\\_download2/various/I2SBUS.pdf](http://www.classic.nxp.com/acrobat_download2/various/I2SBUS.pdf)