Dual XO Clock Board user guide

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Description

The Dual XO Clock Board is a multi-frequency clock board which was designed especially for the I2S FIFO KIT to improve the sound quality and working range by employing two standard clock oscillators. It comes with automatic Fs switching, dedicated low jitter clock fan-out buffers and an enhanced low noise power supply. The Dual XO Clock Board is highly recommended for upgrading the I2S FIFO KIT to achieve higher performance.

KIT includings

- An assembled and tested Dual XO Clock Board (Pb free, double-sided SMT mounting)
- One 6” double-ended U.FL coaxial cable for MCLK output
- One SMT U.FL receptacle (optional used by some applications to connect the MCLK)
- One 2” 10-pin FPC/FFC cable
- Four ¼” rubber rings
- 22.5792 MHz and 24.5760 MHz clock oscillators come installed for function verification

Features and specifications

- Multi-frequency MCLK output capability
- Automatic switching of the MCLK and Fs depending on the input I2S stream
- Low jitter dedicated clock fan-out drivers for better clock quality and isolation
- I2S re-clocking input

  LVTTL (3.3V) input level

  7-pin PH 2.0mm connector
- I2S re-clocking output

  LVTTL (3.3V) logic output level

7-pin PH 2.0mm connector, and

Three 50 ohm U.FL coaxial connectors

Max re-clocking frequency: 550 MHz

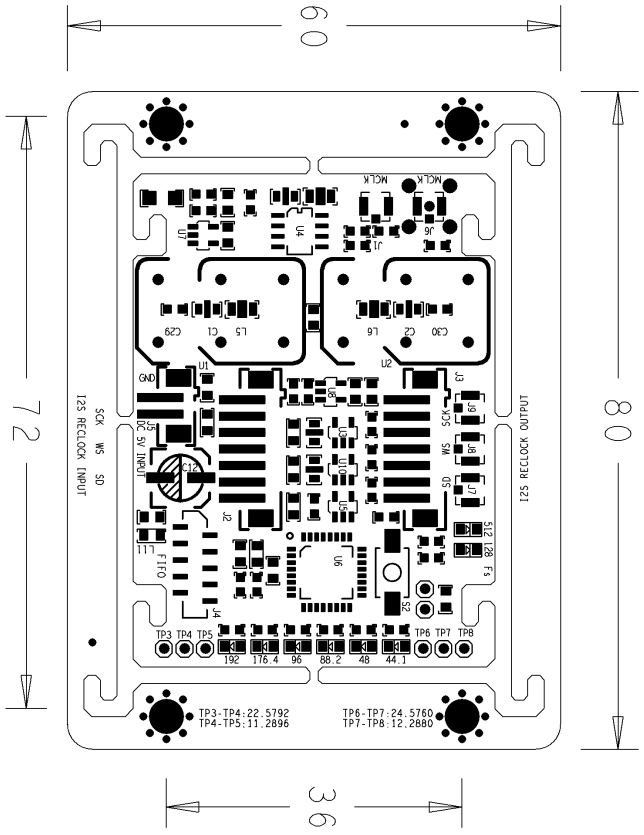
- Power supply

On-board 9µV RMS low-noise, high-PSRR LDOs

Enhanced high performance EMI filters

- Based on standardized interface and protocol, the I2S FIFO KIT can be upgraded seamlessly with the Dual XO Clock Board or other dedicated clock board

Layout and dimensions (in mm)



Connectors and jumpers of the Double XO Clock Board

- MCLK output: J1 and J6, U.FL coaxial cable connectors

- I2S re-clock input: J2, PH 2.0mm 7-pin connector, configured as:

1	2	3	4	5	6	7
GND	SCK	GND	WS	GND	SD	GND

- I2S re-clock output: J3, PH 2.0mm 7-pin connector, configured as:

1	2	3	4	5	6	7
GND	SCK	GND	WS	GND	SD	GND

and, three U.FL coaxial cable connectors, configured as:

J9	J8	J7
SCK	WS	SD

- The Board has two sockets for XOs. Both sockets must be installed with proper XO. Standard DIP 3.3V clock oscillators with 14- or 8- pin configurations are available for U1 and U2

XO socket: U1, a 22.5792 MHz (default) or 11.2896 MHz oscillator should be installed in this socket

XO socket: U2, a 24.5760 MHz (default) or 12.2880 MHz oscillator should be installed in this socket

Once the XOs are chosen, the jumpers have to be set according to the frequency of the XOs, as follows:

TP3, TP4, TP5, frequency setting jumpers for XO in socket U1

U1 frequency	Jumper setting	44.1KHz	88.2 KHz	176.2KHz
22.5792 MHz*	TP3-TP4	512*Fs	256*Fs	128*Fs
11.2896 MHz	TP4-TP5	256*Fs	128*Fs	No support

TP6, TP7, TP8, frequency setting jumper for XO in socket U2

U2 frequency	Jumper setting	48KHz	96 KHz	192 KHz
24.5760 MHz*	TP6-TP7	512*Fs	256*Fs	128*Fs
12.2880 MHz	TP7-TP8	256*Fs	128*Fs	No support

* default

- I2S FIFO board interface: J4, 10-pin FPC/FFC 1.0mm connector, double sided contacts

- J5, Optional DC input (do not use if connected to the FIFO board)

  Optional independent DC power supply for the Dual XO Clock Board. FB L11 has to be removed to use this DC power input. Leave J5 open for normal applications.

- S2, Optional manual frequency setting button. (Not used when the Dual Clock Board is used with the I2S FIFO KIT),

LED indicators

- MCLK frequency indicators:

  512Fs On: MCLK = 512*Fs

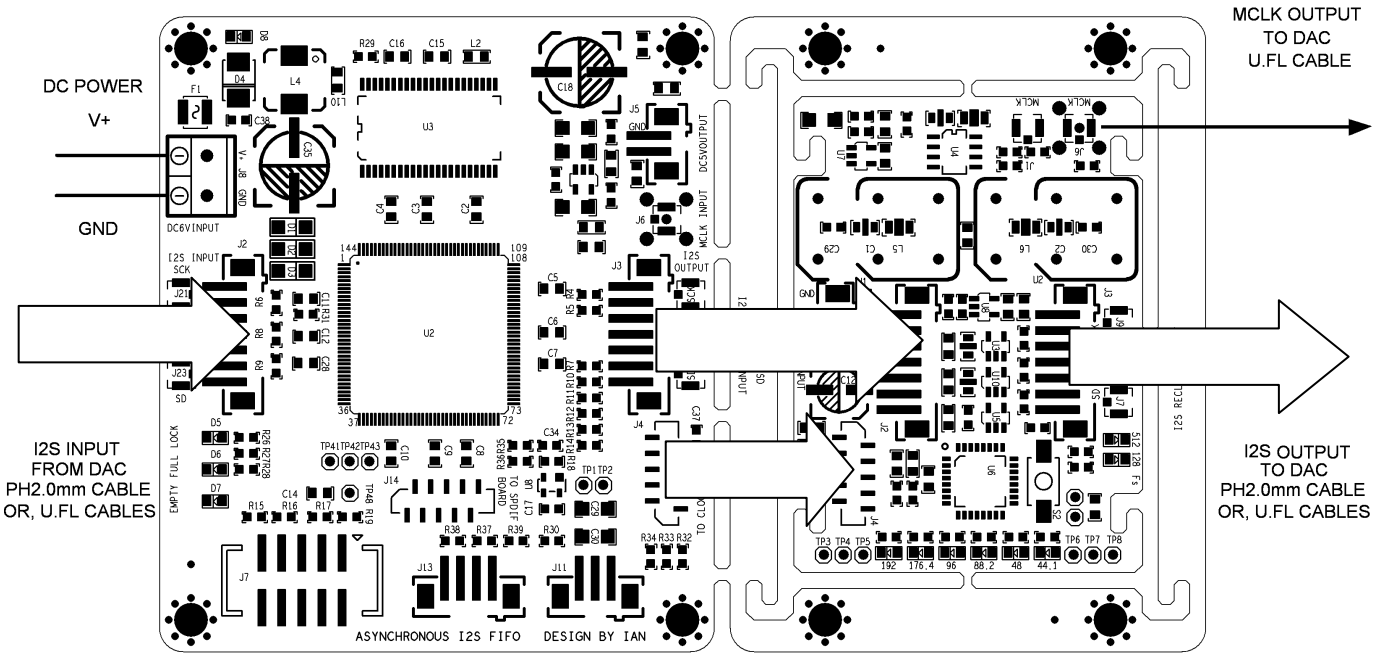
  128Fs On: MCLK = 128*Fs

  Both 512Fs and 128Fs On: MCLK = 256*Fs

- Fs indicators

  44.1 KHz, 48 KHz, 88.2 KHz, 96 KHz ,176.2 KHz, 192 KHz

Upgrading I2S FIFO KIT with the Dual XO Clock Board



1. To replace the Single XO Clock, begin by removing the Single XO Clock Board from the I2S FIFO Kit board by cutting connecting bars along the frame. Similarly, remove the Dual XO Clock from its board by cutting along the frame.

2. Attach the Dual XO Clock to the I2S FIFO Kit board frame with the four rubber rings or just stack it on top of the frame of the I2S FIFO board.

3. The Dual XO Clock must be connected to the I2S FIFO Kit board. Begin by connecting J3 on the I2S FIFO Kit board and J2 on the Dual XO Clock board with the 7-pin PH 2.0mm I2S bridge cable

4. Connect J4 on the I2S FIFO Kit board and J4 on the Dual XO Clock board with the 10-pin FFC/FPC cable, the connectors have double-sided contacts, so the cable can face either up or down
5. Connect the I2S input signals from the DAC or DSP to J2 of the I2S FIFO Kit board using the 7-pin PH 2.0mm cable or the three U.FL coaxial cables to J21, J22 and J23
6. Connect MCLK output from J1 or J6 to the DAC or DSP using the U.FL coaxial cable (J1 and J6 are the same clock signal but come from different drivers)
7. Connect I2S re-clock output signals to the DAC or DSP from J3 on the Dual XO Clock board using the 7-pin PH 2.0mm cable, or from J9, J8, and J7 using three U.FL coaxial cables

Please refer to the user's manual of I2S FIFO KIT for power and other connections

Application notes and tips

- Selection of the XOs

The FIFO itself does not improve the sound, the clocks do. Selecting a pair of really nice low jitter clocks for the Dual XO Clock board is the most important job. The two XO clock oscillators supplied with the board are just generic ones. It is strongly recommended to replace them with better clocks to boost the sound quality. The CCHD-957 series XO oscillators from Crystek have been tested and found to be good choices at a reasonable price. XOs with similar or better phase noise performance are highly recommended. Trying different clock oscillators is an interesting experience.

- Enable pin of the XOs

Many XO oscillators have an enable pin (normally it's pin1 for oscillators with 14- or 8- pin configurations). The output is enabled when the pin is high (> 0.7×Vcc) or open. The output is disabled (High-Z) when the pin is low. If a particular XO is not being selected for MCLK output, the control signal from the socket disables the XO by driving the enable pin low. Usually this does not present a problem because switching between states is very fast. However, some XOs take longer to switch. For example, the Crystek CCHD-957 takes 1 ms. That delay will generate a little switching noise on some DACs. This problem can be solved in one of the following ways:

1. Use the optional SILENCE signal from J12 on the I2S FIFO BOARD to mute the DAC output during the moment of switching;

2. Or just leave the enable pin of that XO open without connecting into the socket.

- Be aware that connecting the XO into the socket incorrectly may damage the XO. Make sure the pin position is correct (pin 1 faces the angled corner).

- Potentials of generic clock oscillators

For some generic clock oscillators, the internal crystal may not be that bad. The problem is usually that generic oscillators do not have a well designed power supply and associated circuit. In many cases, if fed with a high quality, low noise power supply and interfaced with a low jitter output buffer, they will perform better than originally.

- A U.FL tool is recommended to unplug the U.FL cables; otherwise, the connector and the head of the cable could be damaged.

A tool is available here: http://search.digikey.com/us/en/products/U.FL-LP-N-2/H9159-ND/513008

Or you can make one yourself.