SESSION I: ANALOG TECHNIQUES

WAM 1.2: A Bipolar Opamp with a Noise Resistance of less than 50Ω

[See page 286 for Figure 1/Table 1.]

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THE EVER-INCREASING precision of analog circuits demands lower noise in many applications. The $0.9nV/\sqrt{Hz}$ 1kHz noise of the operational amplifier to be discussed is equivalent to the noise of a 50Ω resistor. Consequently, signals in such diverse applications as 350Ω transducer bridges, low-phase-noise frequency synthesizers, and high-quality audio can be amplified with negligible noise contribution from the operational amplifier.

To achieve such low noise requires: *(1)*—an input differential pair of transistors of proper geometry and operating current to support theoretically the noise performance, and (2)—negligible contribution from the rest of the opamp (the input-stage load and second-stage noise sources).

The voltage noise (e_n) of a differential pair of bipolar transistors is given by[1]

$$e_n = \left[8kT\left(\frac{kT}{2qI_c} + r_b\right)\right]^{1/2} \qquad (1)$$

Where: I_c is collector current; r_b is sum of all resistive components, including r_{b1}, the effective pinched base resistance under the emitter; r_{b2} resistance from the edge of the emitter to the base contact, r_{b3} the connecting metal resistances in series with the emitter and base, r_{b4} bond wire and package lead resistances.

The noise equals $0.9nV/\sqrt{Hz}$ at $I_c = 900\mu A$, $r_b = 7\Omega$, $T = 330^\circ K$. The chip temperature will be approximately $30^\circ K$ above the amibient room temperature of $300^\circ K$, because of the relatively high power dissipation (=220mW at ±15V) of the device, necessitated by 1.8mA flowing in the input stage. r_{b1}'s share of the total r_b is approximately 5.5Ω. Each input transistor consists of six 7.5-mil long, 0.7-mil wide emitters. Quad connection effectively doubles the number of emitter stripes to 12; Figure 1. Since the nominal base pinch resistance is 6.5kΩ per square at $\beta = 200$, $T = 330^\circ K$, the input transistor geometry used represents only 0.0008 square of pinch resistance.

The input stage is resistively loaded (R1 through R6 in Figure 2), and the noise of the resistors is $11nV/\sqrt{Hz}$. The sum of the second stage voltage noise and current noise flowing through the load resistors also equals $11nV/\sqrt{Hz}$ at 1kHz; i.e., even the second stage has to be a relatively low noise amplifier by itself. When these noise sources are attenuated by the input stage gain of 100, and is rms summed with the input transistors' noise, the net increase in the total amplifier noise is 1.3%.

At low frequencies, however, the second stage noise is no longer negligible. The culprit is the lateral PNP (Q18, Q19) current noise with its high (500 to 1000Hz) 1/f corner. To minimize this current noise the second stage is operated at only 60% of the input stage current. The double circular structure (Figure 1, at right) maintains high lateral current gain at 550μA of collector current, and also reduces the base resistance of the PNPs. Emitter followers, Q16, Q17 provide a low-source impedance to the lateral current noise. At 5Hz the input-referred noise contribution of the lateral PNPs is $0.7nV/\sqrt{Hz}$. Summed with other less significant 1/f noise components, the overall 1/f corner of voltage noise is at 5Hz; Figure 3.

The base current of the input transistors is nominally 4.5μA with $I_c = 900\mu A$, $\beta = 200$. Bias current cancellation, combined with I_B trimming at wafer sort results in a net input bias current of 15nA, a factor of 300 improvement over the uncanceled current. The current density of transistors Q13 and Q14 matches (Figure 1, right of center) the input transistors Q1 and Q2. Current mirrors Q5 and Q6 invert the base currents of Q13 and Q14 and deliver it to the input. Bias current cancellation is trimmed by adjusting R9. Offset current is not trimmed, but it typically stays below I_B because of the excellent match between Q1 and Q2, Q5 and Q6.

Current noise is that of a pair of transistors operating at 900μA, because bias current cancellation, of course, does not cancel current noise. However, with matched source resistors, bias current cancellation at least does not add to current noise because the current noises in the collectors of Q7 and Q8 are correlated, both originating at the bases of Q13 and Q14.

In most operational amplifiers, the second and third stage operating currents are significantly higher than at the input stage. This permits use of relatively simple frequency compensation because the gain stages do not interact and slew rate is limited by the input stage. In the low-noise design this luxury is not available because of noise and power dissipation constraints. The second stage current is actually lower than the input, and the driver stage is only 30% higher than the input operating current. The five-capacitor/four resistor-frequency compensation network is complex, but it does achieve wide bandwidth, high slew rate and a distortion free output.

Figure 4 shows the wideband noise in the audio range, up to 20kHz: noise is only 0.7μV p-p. Since the output is capable of 25V p-p of undistorted output up to 200kHz, the effective output signal to the input noise ratio in the audio band is 150dB.

Table 1 summarizes specifications achieved: $1nV/\sqrt{Hz}$ noise combined with precision and high-speed performance.

[1] Erdi, G., "Amplifier Techniques for Combining Low Noise, Precision and High Speed Performance", *IEEE Journal of Solid-State Circuits*, Vol. SC-16, p. 653-661; Dec., 1981.

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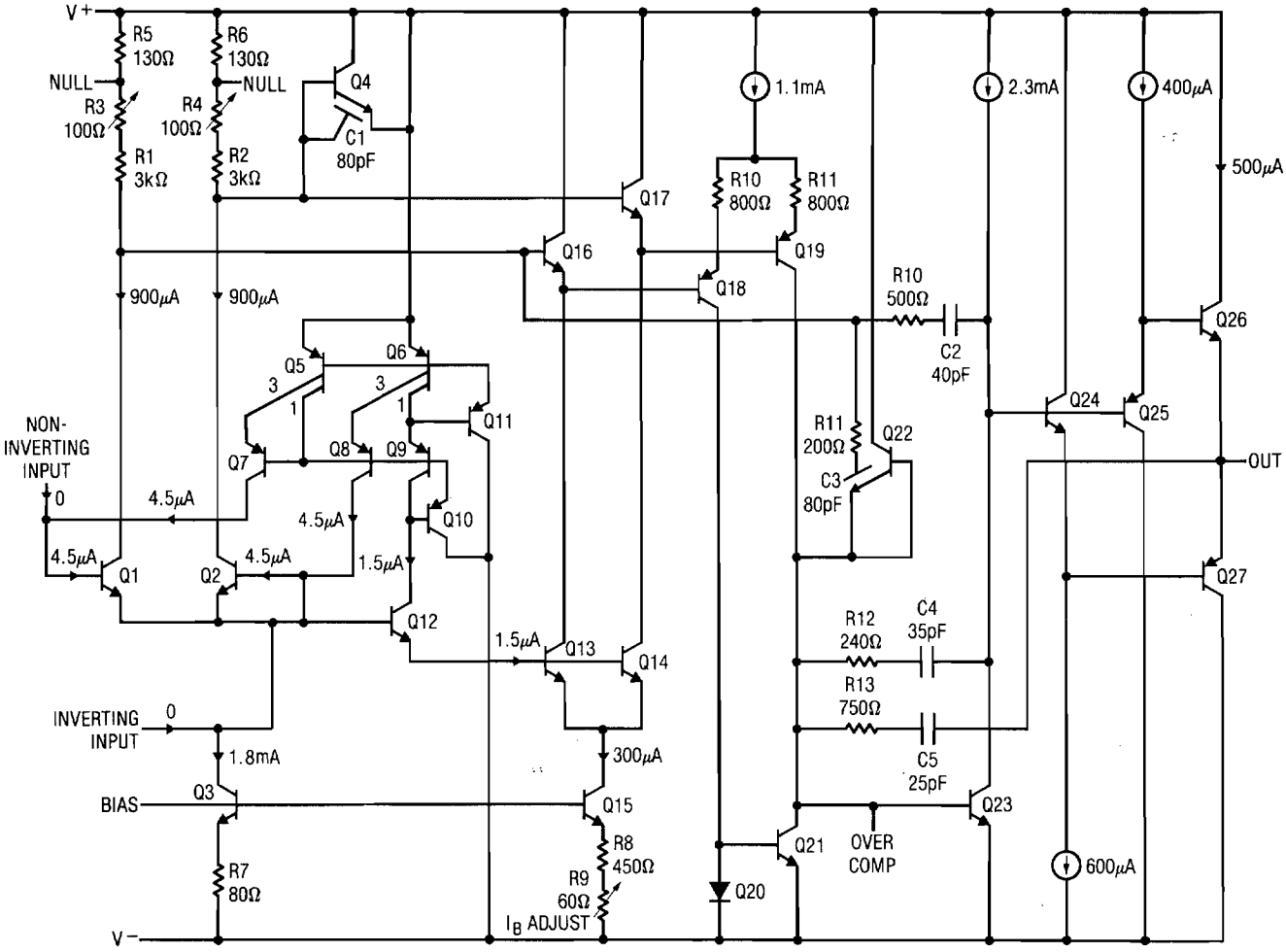

FIGURE 2—Simplified schematic of $1nV/\sqrt{Hz}$ opamp.

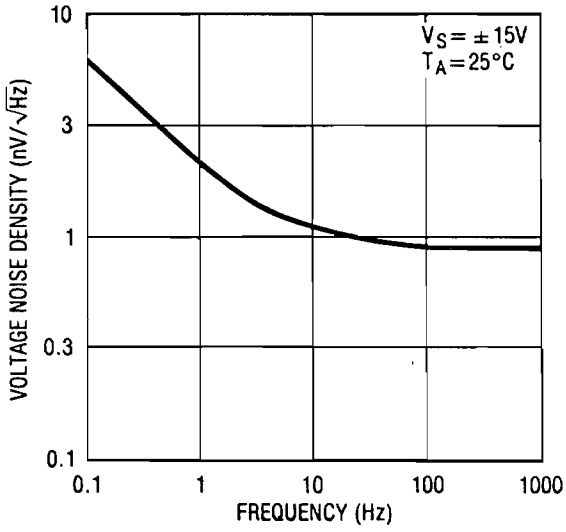

FIGURE 3—Voltage noise spectrum.

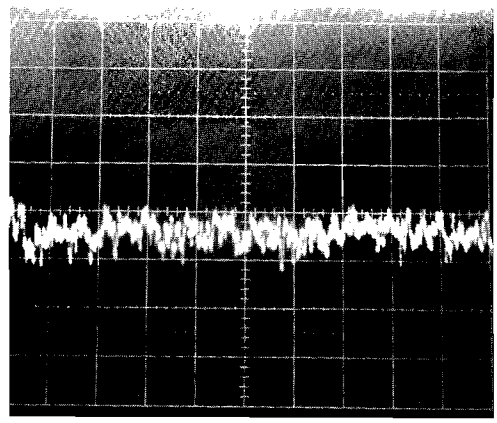

FIGURE 4—Wideband noise to 20kHz: vertical scale = 0.5μV/div.; horizontal scale = 0.5ms/div.

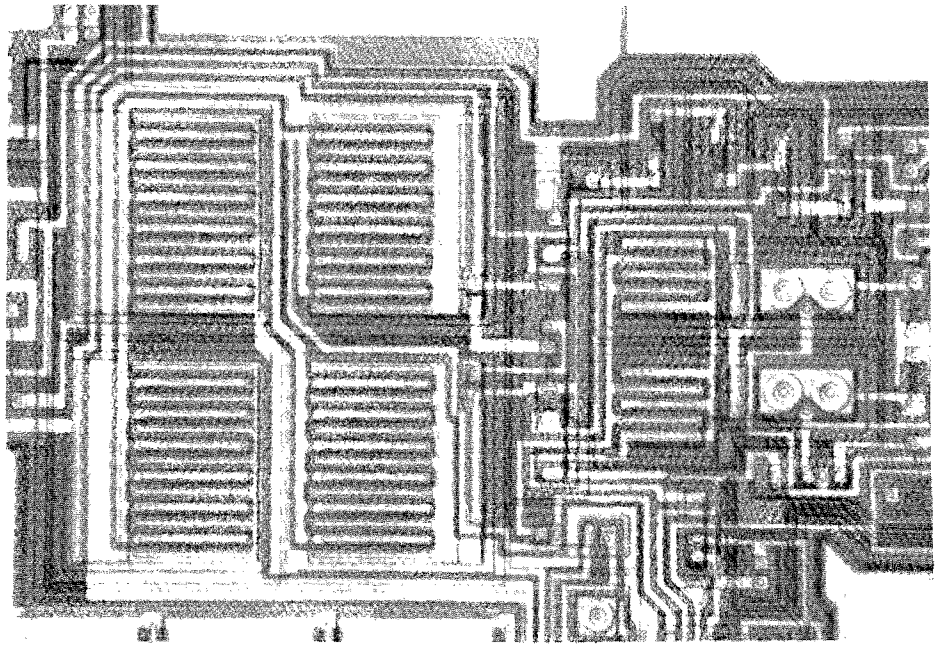

FIGURE 1—Quad-connected, low noise, input transistors: left side of photograph. Bias current cancellation transistors operating at a current density equal to that of the input transistors; right of center. Second stage lateral PNPs; circular structures, at right.

Voltage Noise	f = 1kHz	0.9nV/√Hz
	f = 10Hz	1.1nV/√Hz
	f = 0.1Hz to 10Hz	35nVp-p
Current Noise	f = 1kHz	1.0pA/√Hz
	f = 10Hz	4.5pA/√Hz
Offset Voltage		15μV
Drift with Temperature		0.2μV/°C
Bias Current		15nA
Offset Current		10nA
Voltage Gain: $V_O = \pm 10V$, $R_L = 600\Omega$		5 million
Common Mode Rejection		126dB
Power Supply Rejection		126dB
Supply Current		7.3mA
Slew Rate		15V/μs
Gain Bandwidth Product	f_o = 100kHz	70MHz

TABLE 1—Typical specifications: $V_S = \pm 15V$, $T_A = 25°C$.