

## The DAO SE, an All-FET, Zero- Global-Feedback, Pure Class A Headphone Amplifier (Part 2)

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### Circuitry

#### The standard source follower

The standard JFET source follower has been re-invented for umpteen times. It is essentially a unity gain buffer using two JFETs running at  $I_{dss}$ . The top JFET is the driver and has its drain connected to  $+V_s$ , gate to the input  $V_{in}$ , and source to the output  $V_o$ . This is loaded by a current source connected between  $V_o$  and  $-V_s$ .

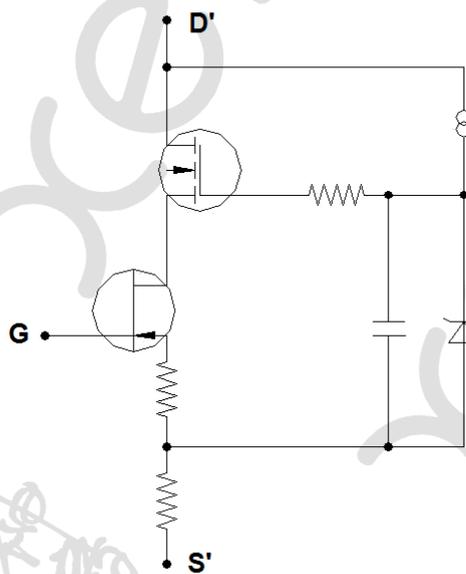
At  $I_{dss}$ ,  $V_{gs}=0$  at both FETs, hence  $V_{in} = V_o$ . The JFET has next to no gate current, and thus provides a high impedance in the mega ohm range. The output impedance of the follower is  $1/Y_{fs}$ , typically between 1 and 40 ohm.

If a pair of well-matched devices of the same type are used in the circuit and are thermally coupled, they will provide very low DC offsets and excellent thermal drift compensation without any adjustment.

One of the most well-known publications of the circuit can be found in "JFETS: The New Frontiers" by Erno Borbely published in Audio Electronics in June 1999.

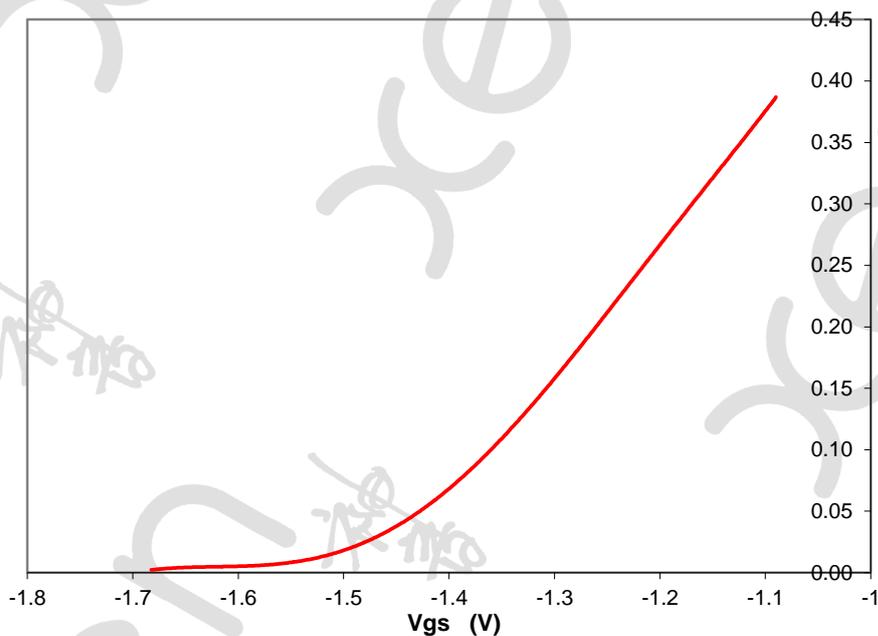
#### The triode cell

The schematic below shows what we named as the JFET triode cell using the LU1014 in modulated cascode mode. This sub-circuit can be treated as a plug-in to replace the "standard" JFET in the traditional source follower, with the exception of course that the  $I_d$  vs.  $V_{gs}$  characteristics follows the triode curve with much better linearity, on top of the LU1014 being cascoded and degenerated, resulting in a much lower effective  $C_{iss}$  and thus allowing higher bandwidth.

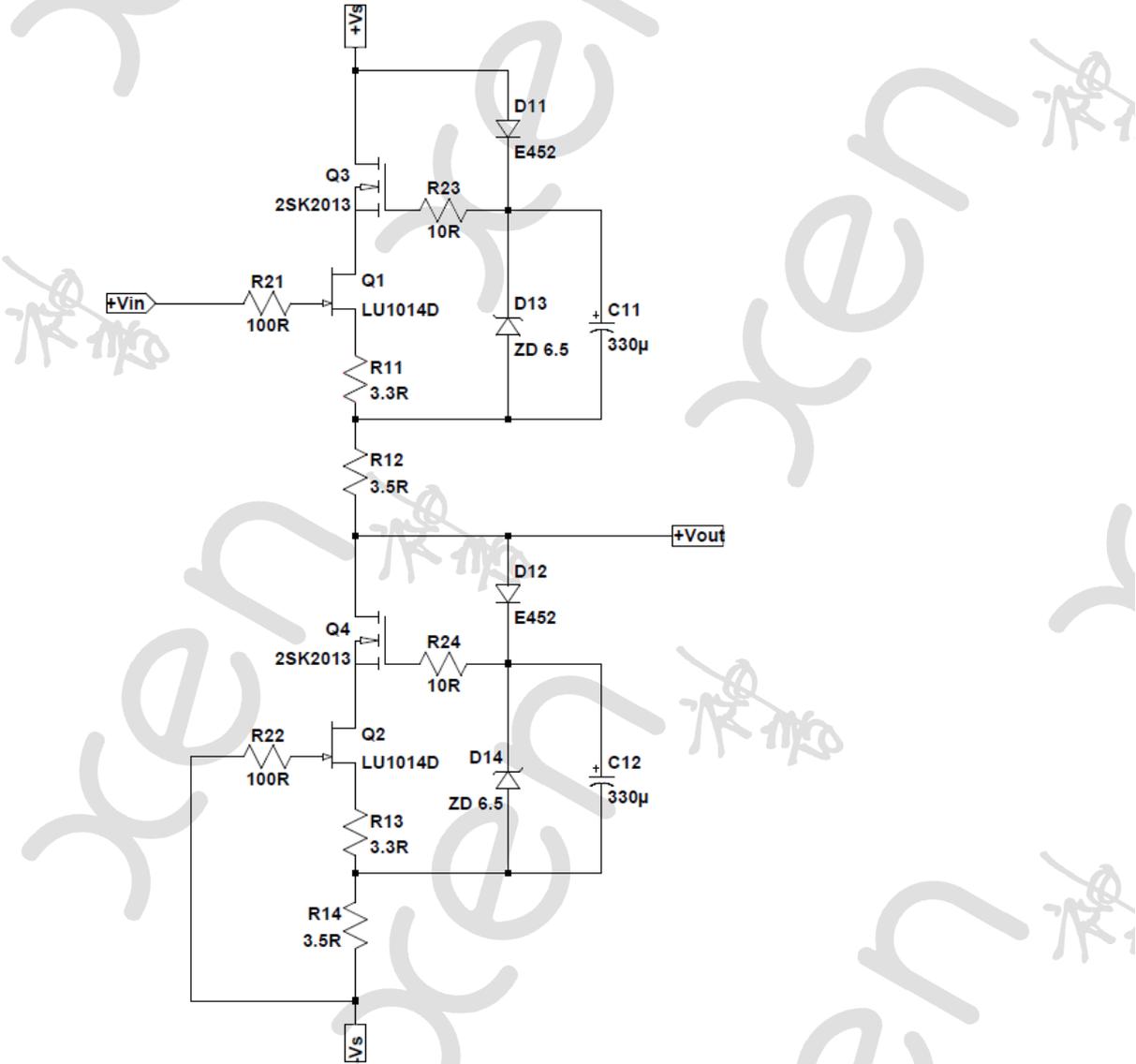


### The JFET Triode Cell

With the appropriate value of  $V_g$  of the cascode devices, as well as source resistors, the LU1014 can be made to operate in triode mode, as shown in the characteristic curve below. Note that this curve represent the actual characteristic of the LU1014 itself, and does not include the additional linearization effect of the two source resistors. The upper source resistor is dimensioned to achieve the right level of  $V_{ds}$  modulation in combination with the  $Y_{fs}$  of the cascode device, whereas the lower resistor is used to set the bias to around 0.2A, i.e. the mid-point of the triode range. Should one wish to use a heavier bias, one only needs to reduce the value of the lower resistor.



If we now take this triode cell and use it to replace the 2 normal JFETs in the source follower circuit, we get the standard configuration of the DAO Power Buffer.



DAO Power Buffer Standard Configuration