



2/28/2003

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## ***Errata: CS8416 Data Sheet Correction***

(Reference CS8416 Data sheet revision DS578PP2)

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- The two sets of external PLL component values listed in Table 2 on page 17 are incorrect. There is only one set of external PLL component values, which cover the entire lock range of 32-192 kHz. The correct external PLL component values are listed below.

Range (kHz)	Rflt	Cflt	Crip	Settling Time
32 - 192	3 k $\Omega$	22 nF	1 nF	4 ms

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### **Contacting Cirrus Logic Support**

For all product questions and inquiries contact a Cirrus Logic Sales Representative.  
To find one nearest you go to [www.cirrus.com](http://www.cirrus.com)

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