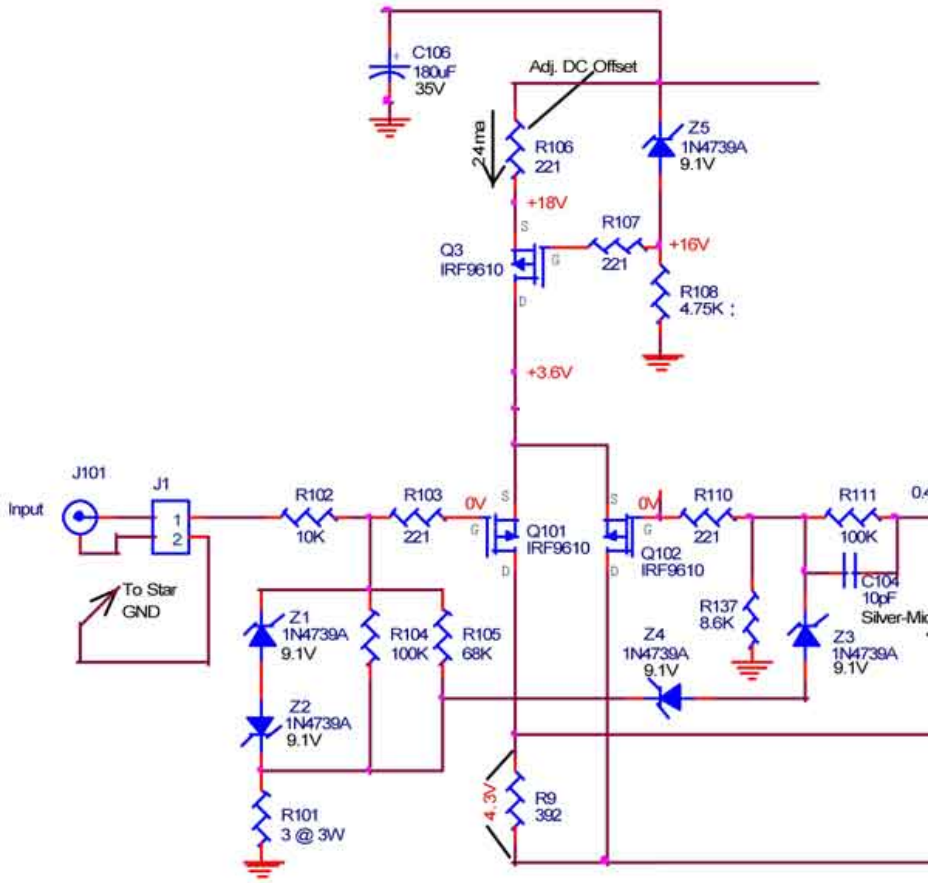
Convert your lousy Aleph to less lousy Babelfish J

There is no easy way for me to make this document, just because my English is not so good…..

Besides that, you must count on few more things : I really don't know much about sand devices….my love is where toobz are……..and –even if I work in repair area for more than 20 yrs , one thing is repairing gadgets, and completely other thing is construction.

Anyway…..good way of starting this (besides repeating my endless mantra how I'm just toob boy wandering through Pass forum) - is to see input stage of plain old Aleph 30:



Just to let you know- this nice pic is ripped from our Diyaudio friend, whose name I always forget; he made, along other nice files, this superb "Aleph30" named pdf file, and signed it as Bergerons. I must give all credits for his nice work.

Alas, you probably have intention to toss out Q101 and Q102, those nasty and crude looking power fets, which only bad designer as Papa is, can put on input of amp. If you have not that intention – why you reading this? Anyway- you also know that their (Q101 and Q102) working point is locked ,defined and baby-sited via Q3

and few parts around it , and all that represents nothing more and nothing less than Constant Current Source ,also known as CCS…..his job is to push 24mA through these crummy input fets ,naturally exactly 24/2 or 12mA through each.

If you have not slightest clue what input differential pair or LTP (Long Tailed Pair) is…….look somewhere at www.passlabs.com in Papa's papers, or somewhere else; I really have not enough mental strength to go soooooo much back in basics….

Ya see that lonely resistor R9? Interesting, laws of physic are again confirmed, 12mA flowing through Q101 also flows through this resistor and somewhat results in voltage potential (across resistor, what else) of approximately 4V3, and that voltage is, again somehow, exactly enough to open enough output mosfet(s).

This is completely possible if we have connected middle point (between Q101 and R9) to gate(s) of output mosfet(s) ……..hehe……

So-how to take out brute mosfets (already placed in input LTP) out and put baby-like delicate j-fets instead?

Easy…..you just need adequate Jfets and enough courage or just enough blessed ignorance to make that in your own…..

Adequate **P-channel** Jfets are exactly ones which can withstand **30V** across drain and source, which can withstand minimum **10mA** in same direction ….or in same path, to be precise more…..

So – you already have in your "Preciousssssss parts" drawer few multileged fuses as 2SJ109BL, 2SJ74BL, say also J176 etc……and you're in game.

If you don't have this-you have problem;

You can solve it in two ways:

1. you can steal , borrow or even buy these little critters ; mebbe is best way to borrow few and never return them ;
2. you can try to find adequate candidates of which I'm not even aware;

So, if you decide to go in honorable path named with No.2, then you must count on another conditio sine qua non, and that 3. condition (besides Uds and Ids already mentioned) is called **transconductance.** That value also illustrate amount of gain you'll have with these jfets in circuit

WTF is this, in fact?

For me-that is one nice characteristic, easy for calculate and understand in toob world. When you take a peek at U-I graph of any toob, you can see how much mA more toob in question will conduct, if you decrease negative voltage on grid for one Volt. So- it's easy – fairy tale thing called **transconductance** is represented in mA/V ;

Catch 22 is that you can't easily take a peek at U-I graphs of multileged fuses, also known as J-fets. Usually their graphs are drawn in some regions not so interesting to us, or they are drawn in inadequate resolution for our needs.

Sometimes you can find transconductance value in datasheets, sometime they're disguised or even not published, so-good luck with finding adequate ones.

Maybe is easiest way for finding good candidates to ask on Diyaudio/Pass for exact types you have in mind ; If your lousy tiny Jfets have just half of

transconductance, comparing to well proven 2SJ109BL , don't despair : you can use two of them ,instead one IRFP……..so- you can use 2+2 instead one 2SJ109BL (which is –in fact-two jfets in one case…..awesome matched, just because both are on same die, substrate, they share same mood, whatever) .

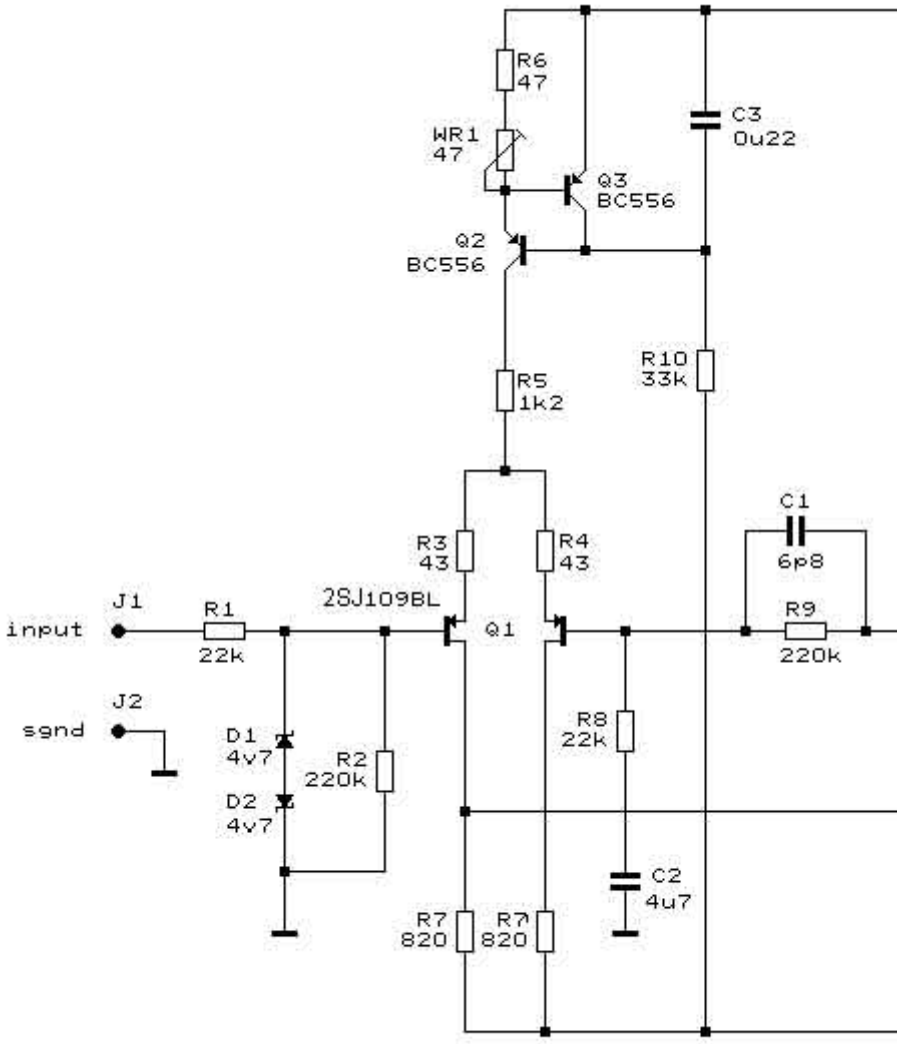
For Jfets matching – chase papers on already mentioned Papa's site or on Diyaudio….

Ok- few hard and sweet and short facts, if you aren't already tired …… :

2SJ109BL : not fried if Uds is bellow 30V ,and Igs is in range to 12 to 13mA per side ; you must also count on max dissipation in each half ,to keep it under 200mW per side……..probably no more than 350mW total . Someone asked for transconductance? Say – in range of 20mA/V , if some ppl aren't lied to me , or I didn't miss-interpret papers .

Everything else you have in (on) mind –you can compare with these values.

To cut long story short , you can look at next picture:



For start – look just at double Jfet (two in one 7-legged case) instead crummy IRFP fets . I hope that is clear .

Second – look at changed value of resistor R7 (in previous scheme R9) ; this change is made because we need to have already mentioned 4V3 across it , and with our ~ 5mA through tiny jfet (value chosen to not burn tiny jfet , and to still have enough muscles to feed gate of output mosfet) value of resistor must be in range of 820 ohms .

Third- R7' is drawn just temporary – later (in full schmtc) you'll see another variation .

Fourth : to have 10mA through Jfet pair (LTP) you can follow two paths:

a) to change R106 in **previous** schematic for string made of 390E resistor and 220E trim pot . Adjusting this for total resistance of 530E before powering up , you'll be in ballpark ,and later you can just readjust to have near zero volts on output of amp

b) you can make "my" version of input CCS (Oly's , in fact ; he drew it,but with R10 ordinary grounded on ground . Grounding it on –Ve and recalculating value was my typicall tweak) and that version is pretty self-explanatory . Before powering up , just adjust WR1 + R6 combo to ~ 60E and you'll be in ballpark of 10mA.
Be sure that you make physical contact between cases of Q2 and Q3 …..just place them tight face to face and wrap them with something. Plastic ties are good for that . R5 is here to take some heat from two sisy bjts…….on his mighty shoulders ;)
Btw. – lower leg of R10 is not grounded on ground ; it's "grounded" " on negative supply , to achieve better CMRR ,at least theoretically.
You don't know what CMRR is? Hehe –that's your problem ,not mine.
You don't need to match these bjts . Use whatever will take 50V and 500mW . Don't ask anyone "can I use xxx instead of yyy", they are all same, if they have enough Beta . "what's beta……" ……

Fifth : R3 and R4 are nothing more than woodoo "source degeneration" ; tool often used to take care of variations between different specimens of used jfets . With them in place , you'll have less gain variations in bunch of 100 pieces 2SJ109….said enough.

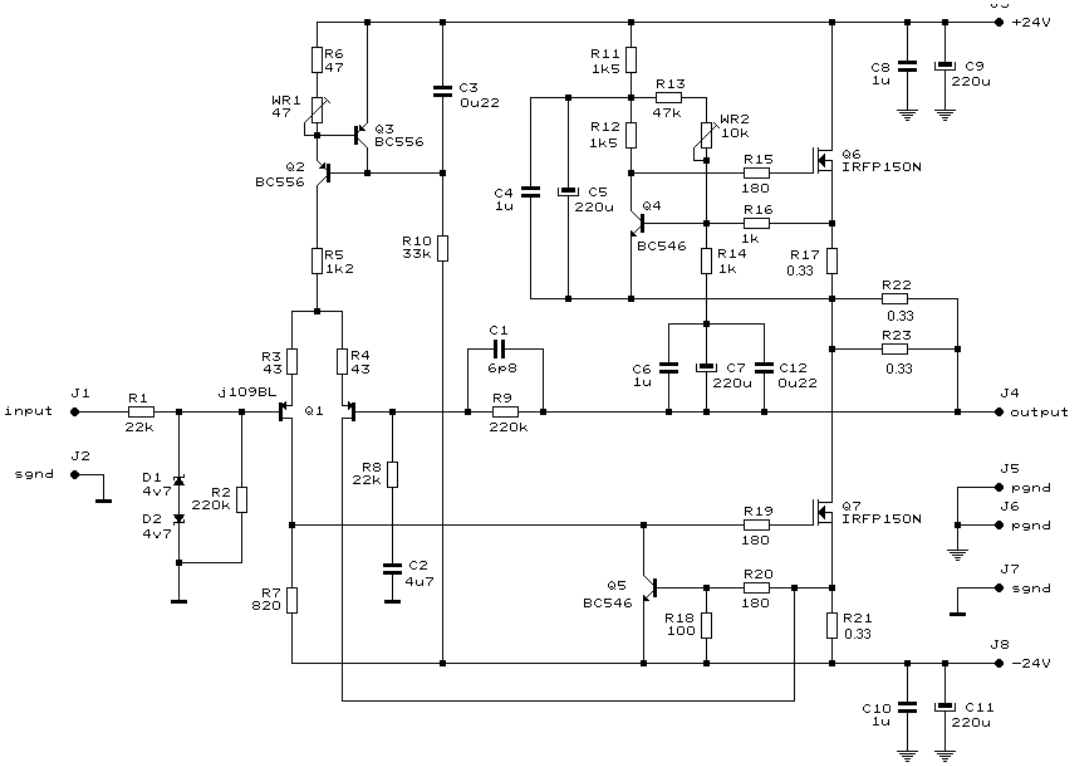
Further :

R1 and R2 are here to tell to your sisy preamp what input impedance it see ;

R8 and R9 are here to define overall gain of amp ; you can use C2 or not (piece of wire instead) – it's here to tell to your amp "do not amplify if some jerk plug 9V battery in input connector ,or some jerk use so sisy preamp which have DC on output".
C1 is here **optionally** if you see weird stuff in squares on your scope during testing . If you have no scope , put it here permanently and sleep well.

Important: For best DC offset control during time (in other words – thermal drift) it's important to have physicaly coupled Jfets (same as two bjts in CCS) – in case that you use two independent Jfets ; in case of dual one (two in same case) it's already done.
Also – best way for soldering any sort of little ones ,and to achieve thermal coupling between them is to make sort of daughter board –with holes for jfets and pins which you'll solder in place of dismantled input mosfets ,with placement adequate for your exact PCB.

OK . there is full Babelfish J schematic ; R7' is gone to the wind, and drain of right Jfet is routed to output mosfet ,to form sorta folded cascode ; weird or not – you can do same or you can just leave R7' in place or you can just route that drain to –Ve .



WR1 – as I said ,is to tweak DC offset on amp output .
WR2 – is there to tweak Iq through output stage ……say – 2A .

Last ……or that need to be first……this funny paper is useful for you if your Aleph have supply up to ± 25VDC . For everything above that (read – any other Aleph iteration) you'll need cascoding for Jfets in range of 30V of Uds……..
Also-count on fact that 5mA through tiny Jfet is good enough for **maximum** 2(two) power mosfets in lower half of amp ; in another words-you can have max two pairs of mosfets per channel .

That’s it .
If I forgot something, forgive me ; it was as creating Ana Karenina to me , writing in non –native language .

All credits to Papa ……he is always amusing and inspirative; this last one-often as stick in your lower back ;) .

Also credits to Mr.Insomnia himself – Gray Rollins …….he gave me few (or more?) valuable tips in my attempts to solve this puzzle .
And-if you see somewhere similar circuit , this is just a sign that this one looks similar to them, not vice-versa …….

And – how close is Babelfish J to Papa’s Aleph J ?
Only Papa can answer to this , and I just can anticipate that he certainly have few details here and there , which can make big or less big difference …….or even lesser difference……

Originall thread is located at
http://www.diyaudio.com/forums/showthread.php?s=&threadid=75281

Zen Mod ……..AKA Choky ……..AKA Prodanovic Aleksandar