ance is infinite, the current required by the circuit elements within block **100** constitute an internal load that bootstraps itself.

J1 is a voltage follower of the output voltage of amplifier A1 and provides base current for Q1. In operation, J1 gate voltage is pulled lower than J1 source voltage by A1 as it nulls the difference around the feedback loop comprised of J1, Q1 and R8. The decrease in J1 gate voltage limits current into Q1 base as the control loop approaches equilibrium. By choosing or designing J1 to have a gate pinch-off voltage Vp of magnitude sufficient to pull error amplifier A1's output below its power supply voltage at node **10**, output voltage VOUT reaches a designed value dependent on the voltage VREF of REF1, an offset voltage VOFS and the ratio of R8/R9 as given by the following equation:

$$VOUT=(VREF*(1+R8/R9))+VOFS$$

In the simplest case, VOFS can be zero volts and VOUT is set as

$$VOUT=VREF*(1+R8/R9)$$

VREF can be generated from a zener or avalanche diode, a band gap reference, a buried zener reference or any other means to generate a fixed reference voltage appropriate to the power supply levels required by A1 and by the desired VOUT.

FIG. **4** is a more detailed embodiment of FIG. **3**. Here, FIG. **3**'s OFFSET element has been replaced by a resistor. PNP emitter follower transistor Q2 has been added to shunt current from the negative supply rail of A1 away from R12. The following analysis ignores the current into the input terminals of error amplifier A1 and the base of Q2 because they are orders of magnitude less than the current through R11, REF1 and R12. VOFS is set by the current through resistor R12 as

$$VOFS=I_{R11}*R12$$

Current through R12 is the sum of currents through resistors R11 and R9. Analysis reveals that the voltage across R11=VOUT-VREF and it can be algebraically deduced from the VOUT equation above that the current I_{R11} through R11 is a fixed value given by

$$I_{R11}=(VREF*(R8/R9))/R11$$

and the current I_{R9} through R9 is a fixed value given by

$$I_{R9}=VREF/R9$$

With a constant known current of $I_{R12}=I_{R9}+I_{R11}$, VOUT can be set to any value below the input voltage VIN minus the dropout voltage of J1 and Q1 by adjusting the value of R12, with the condition that VOUT must be high enough to power A1 and REF1. The circuit comprised of block **100** in FIG. **4** floats at VOFS above a ground reference level, providing output voltage

$$VOUT=VOUTZ+VOFS$$

where

$$VOUTZ=VREF*(1+R8/R9)$$

as given in the simplest case above and

$$VOFS=(VREF*R12/R9)(1+R8/R11)$$

based on the equations for I_{R11} and I_{R9}. With block **100** floating between VOUT and VOFS, only R12 and Q2 need to withstand a high voltage level in the case where VOUT is a large value, allowing most of the circuit to be built from less expensive low voltage elements.

The embodiment of FIG. **4** directly connects both Q1 collector and J1 drain to VIN to yield a dropout voltage of J1 drain to source voltage VDS plus Q1 base to emitter voltage VBE. For a low on-resistance J1 and a typical bipolar power transistor Q1 delivering approximately 10 milliAmps into LOAD, dropout voltage VDS+VBE is between 0.5V and 0.6V, reaching 1.1V to 1.3V while delivering approximately 400 milliAmps into LOAD. The embodiment provides the low output impedance of the bipolar output device Q1, with values in the ones of milliOhms range.

Both J1 and Q1 are unity gain followers, allowing dynamic performance and stability to be governed primarily by error amplifier A1. A1 can be comprised of any suitable difference amplifier such as a differential pair, an operational amplifier (op amp) or an output transconductance amplifier. For stable dynamic performance some op amps require a compensation network CN4 as shown in FIG. **4** which consists of a lead (capacitive) network, but can also be a lag lead (resistive and capacitive) network or Miller capacitance. Depending on the amplifier used for A1, the output may require a dominant pole capacitance to ground to guarantee stability for substantially all load impedances. Added capacitance from the gate to the source of J1 may also be employed to enhance stability for some load impedances.

DESCRIPTIONS OF ADDITIONAL EMBODIMENTS

To limit the output current and thus increase the reliability of the invention, the known current limiting means of foldback current limit discussed in the description of related art can be used. However, to maximize load rejection it is desirable to achieve the lowest possible impedance at the node VOUT. Adding a current sense resistor in series between Q1 emitter and LOAD increases the output impedance by the value of the current sense resistor, which is undesirable.

Adding a resistor between VIN and the drain of J1 is another means to limit Q1 base current, thereby limiting Q1 emitter current to LOAD. This requires a resistance value that depends on the difference in VIN and VOUT , making it difficult to use in a general purpose circuit that can accept a multitude of values for VIN and VOUT.

FIG. **5**

The embodiment of FIG. **5** limits output current with the addition of a depletion mode FET J2 between VIN and J1. J2 limits output current to a value dependent on the pinch-off voltage of J2, without increasing output impedance. Understanding that negligible current flows through the gates of J1 and J2, the shared source to drain current IDS of J2 and J1 substantially constitutes the base current of Q1. With Q1 emitter output current set as beta times Q1 base current, limiting J1 source current limits output current to LOAD. The limit occurs when J1 VDS+Q1 VBE approaches the VGS pinch off voltage of J2. As Q1 base current increases with increasing LOAD current demand, J1 source current increases, simultaneously increasing J1 VDS and decreasing J2 VGS, moving J2 toward pinch off. Pinch off limits source current of J2 and thus J1, limiting current to Q1 base and thus limiting current to LOAD. The circuit in FIG. **5** allows output current limiting while keeping output impedance equal to the lowest possible value, that of a bipolar emitter follower transistor. It has a disadvantage of increasing the dropout voltage by the VDS of J2, which is small at nominal drain current and can be avoided completely by using a separate power supply at the collector of Q1 as with FIG. **6**.

FIG. **6**

Use of a separate power supply VLDO provides the benefit of limiting maximum output current with zero additional output impedance as in FIG. **5**, plus the benefit of even lower dropout voltage. Q1 collector is powered separately with