

metrical shape of the gain-curve of the common-emitter amplifier is mainly determined by the h_{FE} roll-off of the driver- and power transistors.

Table 1. Measured performance versus PSpice simulation.

	PSpice	Measured
Open-loop gain	79dB	77dB
Open-loop -3dB b/w	825Hz	1150Hz
Closed-loop o/p imp. (m Ω)	29	30
Closed-loop o/p imp. 3dB	16kHz	14.5kHz

Mathematical AC analysis of a common-emitter amplifier

In order to gain insight into the common-emitter amplifier, a mathematical AC analysis on a macro model like Fig. A can be used. Frequency-dependent behaviour of the open-loop transfer, the closed-loop output impedance and distortion are studied here.

The macro model of the common-emitter amplifier consists of a voltage to current converter, A_1 , representing the input stage, followed by a current controlled current source, A_2 , representing a two-stage current amplifier.

Miller capacitor C_m connects across the current-gain stage. The dominant source of distortion in A_2 is the current gain dependence of the emitter current - h_{FE} roll-off. This distortion is modelled by a current source connected in parallel with the output current source. The open-loop transfer function of the common-emitter amplifier can be written as,

Residual currents in the output transistors of the common-emitter amplifier are well controlled, see Fig. 4.

As you can see in Fig. 5, the maximum output voltage of the common-emitter amplifier is close to the rail to rail limit. The dissipation of driver and power transistors in overdrive is shown in Fig. 6. This illustrates the low power dissipation of the bias-control loop used in the common-emitter amplifier.

Open-loop gain and phase characteristics, Fig. 7, show a unity gain phase

margin of 45°. The phase margin for β of 1/34 is 85°. Magnitude and phase of the output impedance are given in Fig. 8.

Setting up

We implemented Figure 9 on a pcb, Fig. 10, and used it for measurements.

By adjusting R_7 , the quiescent current of the power transistors $Tr_{11,12}$ was set to 100mA. Note that due to the spread in transistor parameters, a manual control of the quiescent current is necessary. This is usual for power

where,

$$Z_{co} = \frac{1}{G_1 F_1 \beta} \quad (12)$$

$$z_{zc} = \frac{1}{R_p C_m} \quad (13)$$

$$p_{zc} = \frac{1}{\left(\frac{F_1 + 1 - G_1 R_p \beta}{F_1 G_1 \beta} \right) C_m} \quad (14)$$

Closed-loop frequency dependence of the distortion is given by,

$$\frac{V_{out}}{I_d} \propto \frac{1 + \frac{s}{z_{DC}}}{1 + \frac{s}{p_{DC}}} \quad (15)$$