Simulations and measurements

For a 40W/8Ω design of the common-emitter power amplifier of Fig. 2, the supply voltages are: V_p=25V and V_n=–25V. For R_6=100Ω, giving an emitter current of around 6mA, and a Miller capacitor of 1nF, the calculated slew-rate is 6V/μs. The corresponding full-power bandwidth is approximately 40kHz.

We simulated the circuit of Fig. 2 using PSpice. By adjusting R_7 the quiescent current of the power transistors Tr_{11} and Tr_{12} was set to 100mA.

Using equation (4), the peak output current is approximately 20A. The closed-loop voltage-gain of the circuit is depicted in **Fig. 3**. The nearly sym-

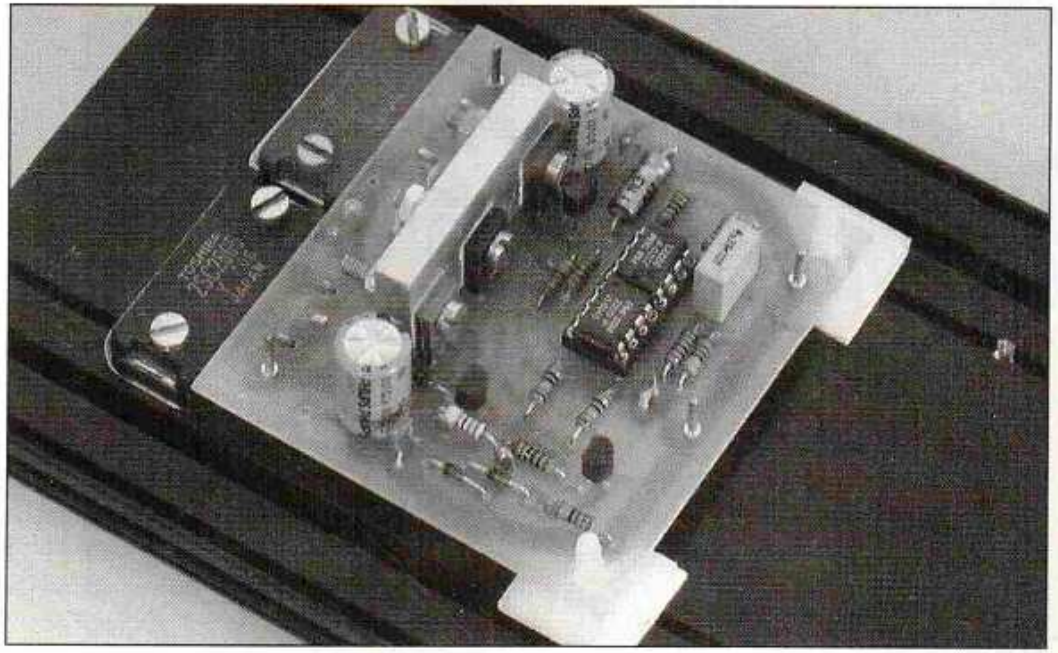
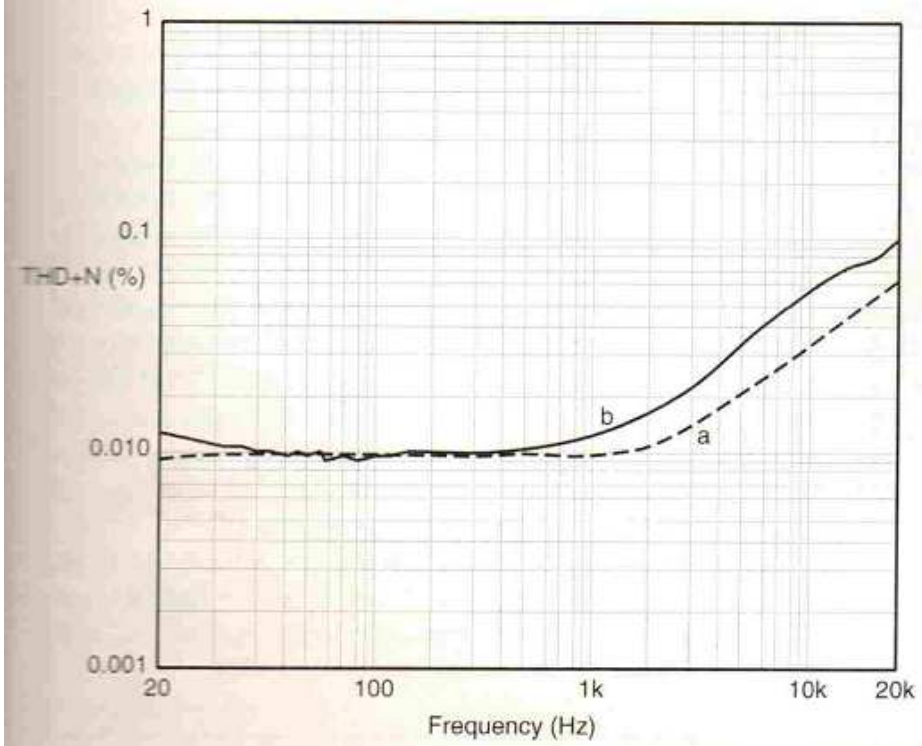


Fig. 10. The authors' prototype amplifier.



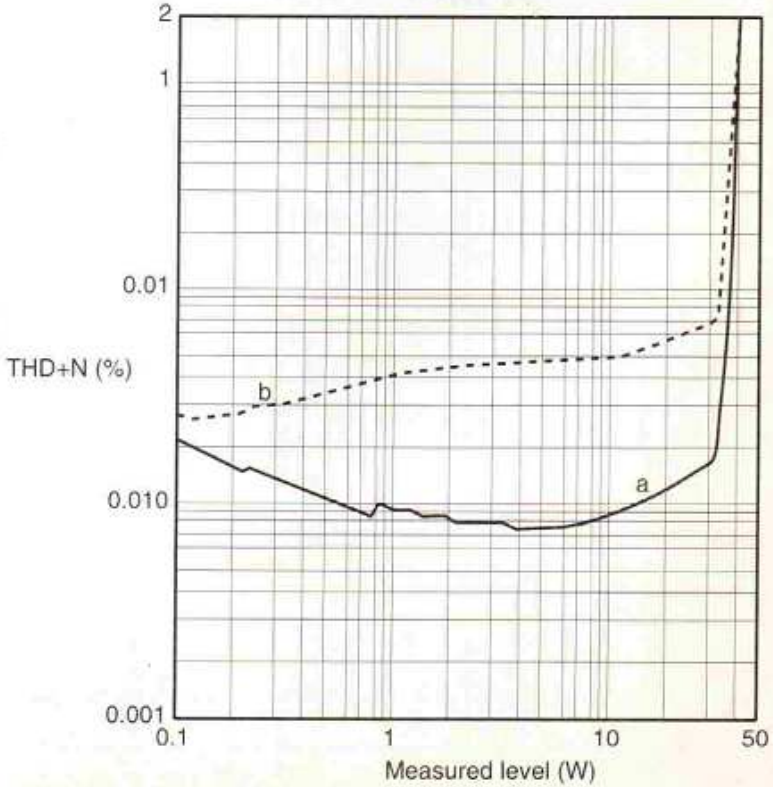


Fig. 11. Measurement of THD+noise versus frequency, a), and THD+noise versus level in watts, b). Curve a in a) is 1W, b is 30W. In b) on the right, a is 1kHz and b is 10kHz.