is approximately 0.6%/K[4]. Maximum output current is determined by emitter current and the current gain of $Tr_{9,11}$ or $Tr_{10,12}$ respectively,

$$I_{O(\max)} = \pm I_E h_{FE}^2 \quad (4)$$

It can be seen that, in contrast with many other designs, the maximum output current capability is symmetrical.

Optimisation

Figure 2 shows the complete amplifier as used for our PSpice simulations. Adding Tr_5 simplifies equation (3) to,

$$I_{C9}=I_{C10}=I_R \quad (5)$$

As a result, the quiescent current of the output stage is,

$$I_{C11}=I_{C12}=h_{FE}\times I_R \quad (6)$$

Note that the maximum available base current for Tr_8 is increased with a factor square-root h_{FE} and the accuracy of the bias control loop is increased too.

Capacitors C_m and C_f perform frequency compensation. Capacitor C_m is a Miller capacitor, compelling the open-loop transfer to a first-order frequency behaviour. Capacitor C_f forms feed-forward frequency compensation around the common-base connected level-shift transistor Tr_8.

Currents I_E and I_R are determined by V_{diode}/R_6 and V_{diode}/R_7 respectively. Emitter degeneration – R_1 and R_2 added to Tr_1 and Tr_2 respectively – is used to increase the amplifier's input voltage range to reduce transient intermodulation distortion.

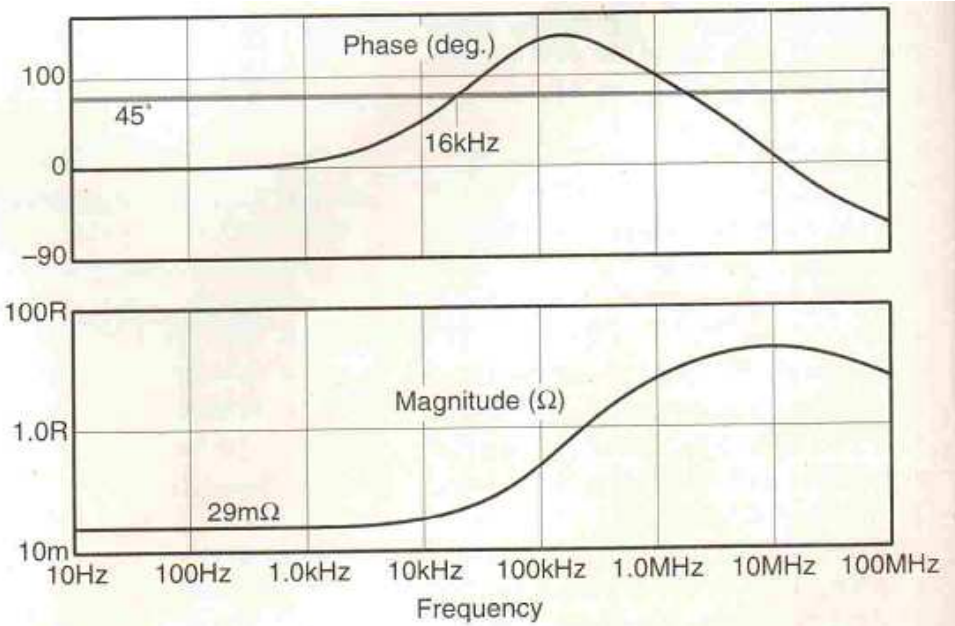

Fig. 8. Magnitude and phase plots of the output impedance.