This started out as an exercise in the design of a discrete op-amp using up to date readily available components and put the design into the creative commons. This version has an added aspect. It is an attempt to get the most out of a single gain stage and buffer. This gives us the opportunity to put the compensation capacitance to ground. The typical VAS and pole splitting capacitor can present an opportunity for supply noise to enter the signal path. It also offers the user a very easy platform for playing with gain bandwidth product (GBW) and open-loop bandwidth.

The input stage

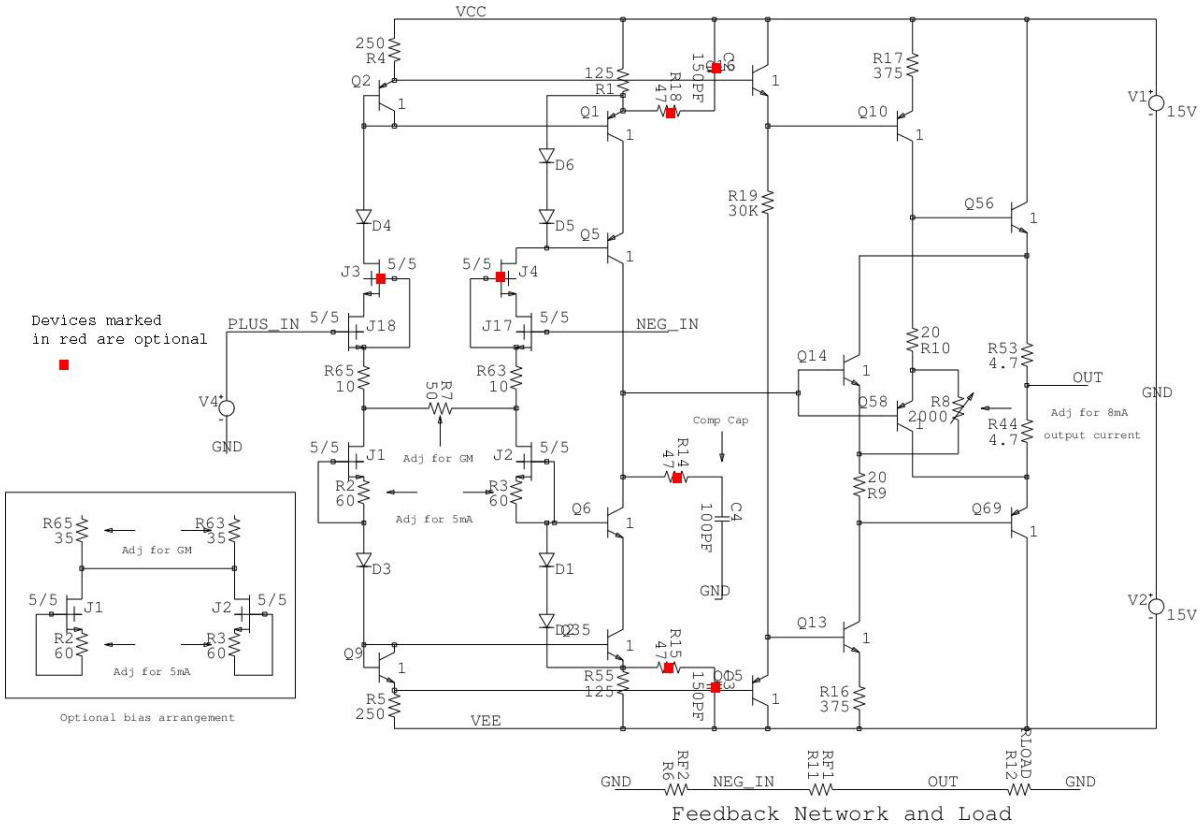
The input stage looks on the surface similar to some previous designs such as those from Hafler. In those designs what looks like a folded cascode is in reality a cascade of a resistively loaded long-tailed pair and a common emitter VAS. The input pair effectively is used as a single ended gain stage. Here the input sees a true folded cascode where the two sides of the input pair contribute equally to the output current. JFET's were chosen for their low input current and more linear transfer function. They also have a favorable tradeoff between open loop bandwidth and slew rate since they have less transconductance (gm) than bi-polars at high current. The input is operated at 5mA per side which gives a net transconductance (degeneration resistance plus the JFET's gm) of around 1/100 Ohms (.01 S). This and 100pF compensation capacitance gives around a 32 MHz GBW (2*gm/(2pi*C)) which is reasonable for a large range of discrete devices including some high voltage types that tend to have lower ft's. At higher closed-loop gains the compensation capacitance and/or the degeneration resistors (R65,63,7) can be reduced, lowering distortion without inducing oscillation. The circuit as shown is stable at gains of 5 and

above, the passive components marked in red can be used for closed-loop gains down to 1. These are suggested values. The exact values will depend on the devices chosen.

One of the issues with using a single gain stage is that any current errors at the output will reflect directly to the input which can cause distortion. Here cascode devices Q5 and Q6 have their base currents recaptured into the emitters of Q1 and Q35. At high frequencies the base currents have a non-linear component due to the Ccb. This technique also works at DC so the open-loop gain can reach 120dB. The lower bias arrangement might seem like obsessive mirror imaging, but this is one way of exactly duplicating the dynamic base current recapture.

Output stage

As stated the output stage must present minimal input current deviations with voltage and load. This is mainly accomplished by bootstrapping the collectors of Q14 and Q58. This version of the amplifier is designed for a 600 Ohm load and at 8mA of bias the output stage never switches off in either direction and the total amplifier supply current stays at around 25mA which should be low enough in retrofit applications without the need to increase the power supply capacity. The output stage needs two current sources for bias (Q10, Q13). These are set by tapping voltages off at R4 and R5. This voltage is set by the input bias current so this remains the sole reference source for the entire circuit. There is an additional benefit in that during slew there is a feedforward path all the way to the bases of the output transistors.


VCC
250
R4
Q2
125
R1
Q1
C2
150PF
R18
47
Q10
R17
375
V1
15V
D6
D4
D5
Q5
R19
30K
Q56
J3
5/5
J4
Devices marked
in red are optional
PLUS_IN
J18
J17
NEG_IN
R65
10
R63
10
R7
50
Q14
20
R10
R53
4.7
OUT
GND
Q58
R8
2000
Adj for 8mA
output current
R44
4.7
V4
GND
Adj for GM
J1
J2
Comp Cap
R14
47
R2
60
R3
60
Adj for 5mA
Q6
C4
100PF
20
R9
Q69
D3
D1
D2
D5
Q13
V2
15V
Q9
R15
47
R55
125
Q3
150PF
R16
375
R5
250
VEE
GND
RF2
R6
NEG_IN
RF1
R11
OUT
RLOAD
R12
GND
Feedback Network and Load
R65
35
R63
35
Adj for GM
J1
J2
R2
60
R3
60
Adj for 5mA
Optional bias arrangement