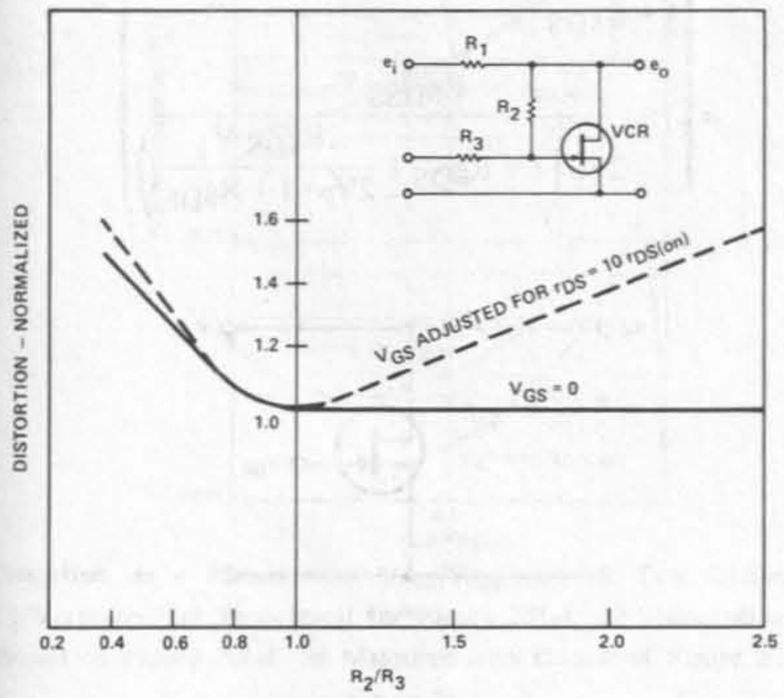
Some degree of non-linearity will be experienced in both the first and third quadrants as $V_{GS}$ approaches the FET cut-off voltage. For this reason, it is important that the feedback resistors be of equal value so that the non-linearities likewise will be equal in both quadrants. Figure 24 shows a curve of distortion vs $R_2/R_3$, in both quadrants.




**Distortion vs $R_2/R_3$**
**Figure 24**

Distortion resulting from changes in temperature are also minimized by the feedback resistor technique. $r_{DS}$ will change with temperature in an inverse manner to the behavior of FET drain current. Table I presents the result of VCR laboratory performance tests of distortion vs temperature. The VCR7N again was employed. Signal level was 2 V peak-to-peak.

**Table I**

| Temperature (°C) | Without Feedback | | With Feedback | |
|---|---|---|---|---|
| | $r_{DS} = r_{DS(on)}$ | $r_{DS} = 10\ r_{DS(on)}$ | $r_{DS} = r_{DS(on)}$ | $r_{DS} = 10\ r_{DS(on)}$ |
| +125 | >13% | >6% | <0.5% | <0.5% |
| + 25 | >10% | >5% | <0.5% | <0.5% |
| – 55 | 3.9% | 3.2% | <0.5% | <0.5% |

## *SUMMARY*

This Application Note has presented a brief description of the use of junction field-effect transistors as voltage-controlled resistors, including details of operation, characteristics, limitations, and applications. The VCR is capable of operation as a symmetrical resistor with no DC bias voltage in the signal loop, an ideal characteristic for many applications.

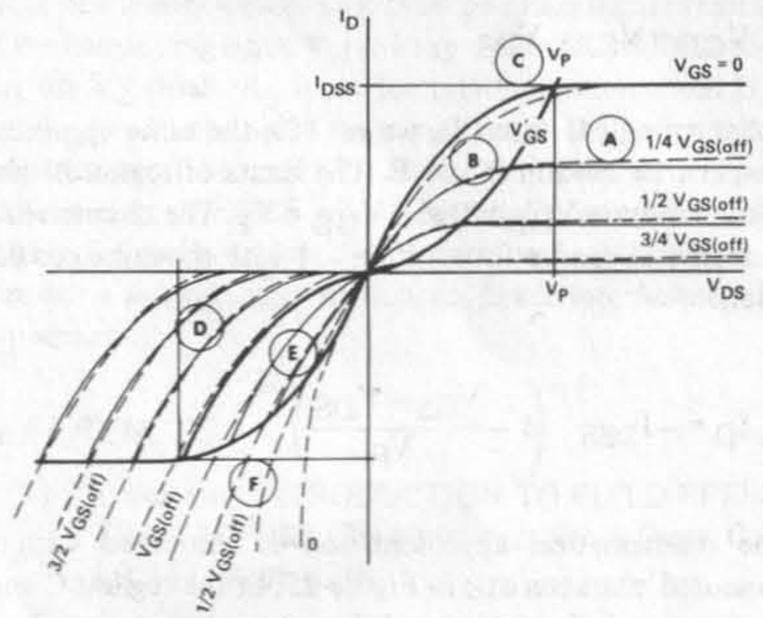
Where large signal-handling capability and minimum distortion are system requirements, the feedback neutralization technique for VCRs is an important tool in achieving either or both ends.

It has also been shown that FETs with high pinch-off voltage require larger drain-to-source voltages to produce drain current saturation. Therefore, FETs with high $V_{GS(off)}$ will have a larger dynamic range in terms of applied signal amplitude, while maintaining a linear resistance. It is advantageous to select FETs with high $V_{GS(off)}$ (compatible with the desired $r_{DS}$ value) if large signal levels are to be encountered.

## *APPENDIX A* – From proceedings of the IEEE, October, 1968, pp. 1718-1719.

Abstract – An analytical approximation of FET characteristics for positive and negative voltages is presented. The distortion in an application as a controlled attenuator is calculated, and a method of reducing distortion by a factor of more than 50 is described.

Controlled resistors are used in oscillators, controlled amplifiers, and attenuators.[6,7] The possible control range is much larger for field-effect transistors (FET) than for other elements with comparable time constants (e.g., diodes). The signal-to-noise ratio is considerably improved.




**Comparison Between Mathematical Approximation of FET Characteristics (Solid Lines) and Measured Curves (Broken Lines) for a Typical N-Channel JFET**
**Figure 25**

Figure 25 shows idealized and real FET characteristics. In region A (above pinch-off) $I_D$ is independent of $V_{DS}$:[8]

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad (1)$$

Region B, where $V_{DS} < (V_{GS} - V_P)$, is the so-called triode region. (In the following discussion all the signs (+, –) will be valid for N-Channel FETs.) The characteristics can be

5

approximated by a quadratic function, of which the maximum and a second point (the origin) are known. The approximation is

$$I_D = I_{DSS}\left[\left(1-\frac{V_{GS}}{V_P}\right)^2-\left(1-\frac{V_{GS}-V_{DS}}{V_P}\right)^2\right]$$

$$=\frac{2I_{DSS}}{(V_P)^2}\ V_{DS}\left(V_{GS}-V_P-\frac{V_{DS}}{2}\right) \qquad (2)$$

This is the same function that can be found by a simple analysis based on semiconductor theory. The less negative of the two voltages across the junction ($V_{GS}$, $V_{GD}$) controls the channel conductance. Under the condition that the FET is symmetrical (drain and source interchangeable), the following consideration is true. If $V_{GD}$ were the controlling voltage and $V_{DS} < 0$, $I_D < 0$, then the characteristics would be the same as in the first quadrant:

$$-I_D = -\frac{2I_{DSS}}{V^2_P}\ V_{DS}\left(V_{GD}-V_P+\frac{V_{DS}}{2}\right) \qquad (3)$$

Since the controlling voltage for both regions (B and E) is $V_{GS}$,

$$V_{GD} = V_{GS} - V_{DS} \qquad (4)$$

Substituting (4) into (3), we get (2); the same approximation can be used in B and E. The limits of region E where (2) is valid are $V_{GD} = 0$ and $V_{GD} = V_P$. The characteristics in region D can be found from (1) with the same consideration:

$$I_D = -I_{DSS}\left(1-\frac{V_{GS}-V_{DS}}{V_P}\right)^2 \qquad (5)$$

The mathematical approximation is compared with the measured characteristic in Figure 25. In the regions C and F the junction is forward biased. The characteristics are dependent on the internal resistance of the gate voltage source since gate current flows.

The FET as a controlled resistor works in region B and E. The higher the resistance, the more non-linear are the characteristics. For most applications this is undesirable. Based on the simple approximation (2), the relation between distortion, control range, and maximum to minimum attenuation will be described for a simple voltage divider [Figure 26(a)]. Most applications can be based on this simple example. The conductance in any point of region B or E is

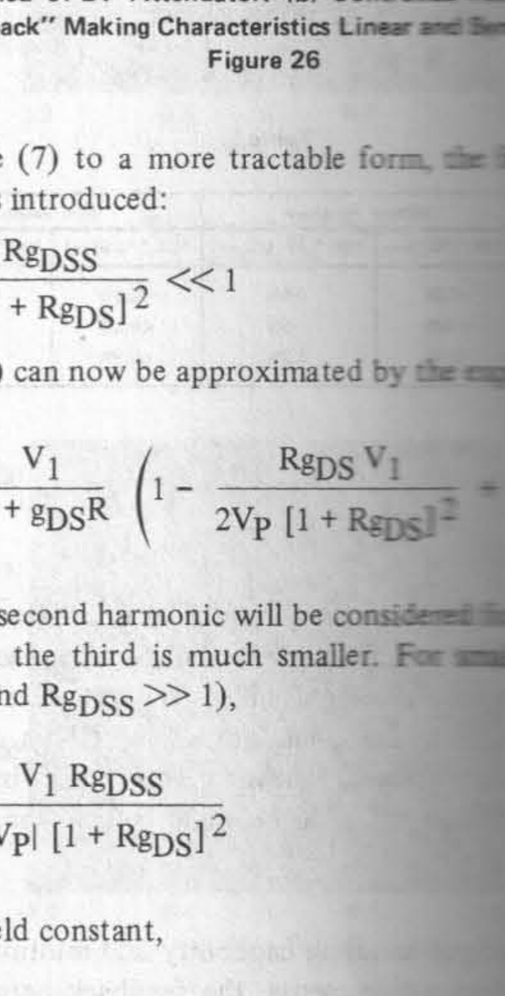
$$G_{DS} = \frac{I_D}{V_{DS}} = -\frac{2I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$$

$$-\frac{I_{DSS}}{(V_P)^2}\ V_{DS} = g_{DS} + \frac{g_{DSS}V_{DS}}{2V_P} \qquad (6)$$

where $g_{DS}$ is the differential conductance at the origin when $V_{GS} = 0$, then $g_{DS} = g_{DSS}$. The attenuation for the circuit of Figure 26(a) is

$$\frac{V_2}{V_1} = \frac{1}{1+Rg_{DS}}$$

$$= \left[\begin{array}{l} 1 + Rg_{DS} \\ \quad + \dfrac{Rg_{DSS}\,V_1}{2V_P\left(1+Rg_{DS}+\dfrac{2Rg_{DS}\,V_1}{2V_P\,(1+Rg_{DS})}\right.} \end{array}\right]^{-1}$$




**(a) Controlled JFET Attenuator. (b) Controlled Attenuator with "Feedback" Making Characteristics Linear and Symmetrical**
**Figure 26**

To reduce (7) to a more tractable form, the following equality is introduced:

$$\frac{V_1\,Rg_{DSS}}{2V_P\,[1+Rg_{DS}]^2} \ll 1$$

so that (7) can now be approximated by the equation

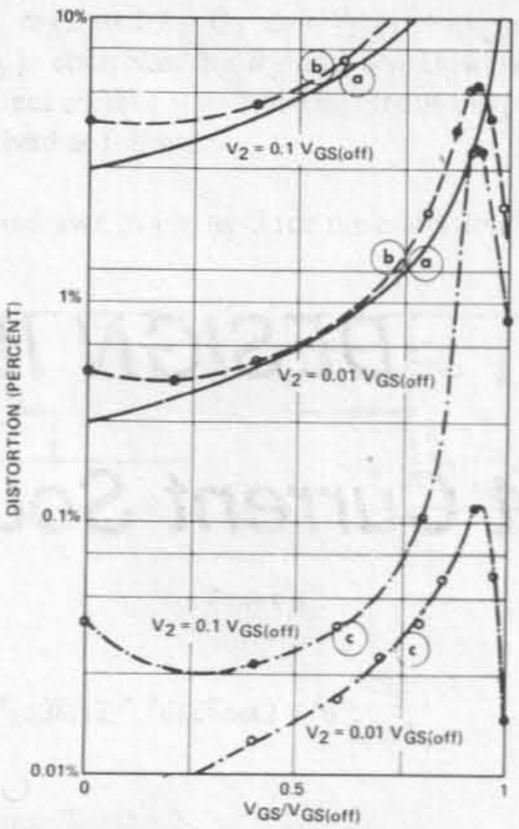
$$V_2 = \frac{V_1}{1+g_{DS}R}\left(1-\frac{Rg_{DS}\,V_1}{2V_P\,[1+Rg_{DS}]^2}+\ldots\right.$$

Only the second harmonic will be considered for the distortion since the third is much smaller. For small distortion ($d \ll 1$ and $Rg_{DSS} \gg 1$),

$$d = \frac{V_1\,Rg_{DSS}}{4\,|V_P|\,[1+Rg_{DS}]^2}$$

If $V_2$ is held constant,

$$d = \frac{V_2\,Rg_{DS}}{4\,|V_P|\,[1+Rg_{DS}]} \approx \frac{V_2}{4\,|V_P - V_{GS}}$$




**Distortion as a Function of $V_{GS}/V_{GS(off)}$ for Two Different $V_2/V_{GS(off)}$. (a) Theoretical for Figure 26(a). (b) Measured with Circuit of Figure 26(a). (c) Measured with Circuit of Figure 26(b)**

**Figure 27**

Figure 27 shows a comparison of measured and calculated distortion. If $V_{GS}$ approaches $V_P$, the above restrictions are violated; the expression for the distortion can no longer be applied. If $V_{DS} < 0$, $V_{GS} = 0$, then the FET works in region F; the distortion will be higher than predicted. From (10) we get for a prescribed maximum distortion a maximum amplitude as a function of $V_{GS}$:

$$V_{2max} = 4d_{max} |V_P - V_{GS}| \tag{11}$$

For a given $d_{max}$ and $V_{2max}$ the ratio of minimum to maximum attenuation is

$$\frac{A_{min}}{A_{max}} = m = \frac{1 + Rg_{DSS}}{1 + Rg_{DSS} \dfrac{V_{2max}}{4d_{max} |V_P|}} \approx \frac{4d_{max} |V_P|}{V_{2max}} \tag{12}$$

valid only for $m > 1$. Note that the maximum distortion is reached only for minimum attenuation. Examples:

$d_{max}$ = 10 percent $V_{2max} = 0.001\ V_P$ $m = 400$

$d_{max}$ = 1 percent $V_{2max} = 0.01\ V_P$ $m = 4$

Although these relations are only first-order approximations, they give a good estimate of FET attenuator characteristics. The maximum amplitude is proportional to $V_P$. FETs with high $V_P$ are desirable for attenuator applications. Unfortunately, the majority of commercially available FETs are made with low $V_P$ for use in amplifiers.

There are several means of reducing distortion. By connecting two identical FETs in antiparallel or antiseries, nonlinearities can be cancelled out to a certain extent. A better linearization is possible by using one FET with "feedback". It has been shown above that the characteristics would be symmetrical if $V_{GD}$ were the control voltage in the third quadrant. By adding 0.5 $V_{DS}$ to the control voltage, the two voltage $V_{GS}$ and $V_{GD}$ interchange when $V_{DS}$ changes sign:

$$\begin{aligned} V_{GS} &= V_H + 0.5\ V_{DS} \\ V_{GD} &= V_H - 0.5\ V_{DS} \end{aligned} \tag{13}$$

then (13) used in (2) gives

$$I_D = \frac{2I_{DSS}}{V^2_P}\ V_{DS}\,(V_H - V_P) \tag{14}$$

The resulting characteristic is linear and symmetrical in B and E. The improvement in distortion performance can be seen in Figure 27. A distortion of 12 percent for $V_2 = 0.1\ V_P$ at $V_{GS} = 0.8\ V_P$ is reduced through linearization to 0.1 percent. Figure 26(b) shows a possible circuit. The frequency range of the controlled signal must be much higher than that of the controlling signal $V_H$ to keep the direct interference of $V_H$ on $V_2$ small. $R_3$ is set for minimum distortion. If $V_2$ and $V_H$ are in the same frequency range, a high impedance amplifier must be used. $V_2$ is at the input; the output is connected to the FET gate. The amplification is approximately 0.5 (adjustable). The control voltage is introduced through a second input so that no direct interference with $V_2$ occurs.

## *REFERENCES*


(1) J. Watson, INTRODUCTION TO FIELD-EFFECT TRANSISTORS, Siliconix, Inc. Santa Clara, Calif. 95054 (1970), p. 58.

(2) "FETs As Voltage-Variable Resistors," Carl D. Todd, ELECTRONIC DESIGN, Sept. 13, 1965, pp. 66-69.

(3) Op. cit., AN INTRODUCTION TO FIELD-EFFECT TRANSISTORS, p. 22.

(4) "FETs As Voltage-Controlled Resistors," Siliconix, inc., Santa Clara, Calif., 1966.

(5) Op. cit., AN INTRODUCTION TO FIELD-EFFECT TRANSISTORS, p. 61.

(6) W. Gosling, "Voltage Controlled Attenuators Using Field-Effect Transistors," IEEE Trans Audio, Vol. AU-13, pp. 112-120, Sept.-Oct., 1965.

(7) J.S. Sherwin, "Voltage Controlled Resistors (FET)," Solid State Design, pp. 12-14, Aug. 1965.

(8) L.J. Sevin, "Field-Effect Transistors," New York, McGraw-Hill, 1965.