# Advanced re-clocking for TDA1541 based CD players

A basic clock upgrade will replace the standard clock (XTAL) with a low jitter high quality item such as the Audioupgrades.co.uk C1 or C2 clock. This upgrade will provide a marked improvement in audio accuracy (clock jitter errors) and therefore sound quality. Further marked improvements can be made if you provide the upgrade clock with its own very low noise power supply. This is what most clock upgrade manufacturers and suppliers consider when're-clocking' the player.

One of the limitations of a basic clock upgrade is that the clean clock will only replace the single clock feed to the original clock distribution device (in this case the digital filter chip primarily responsible for signal oversampling). There will be other devices within the player that require some form of related clock signal. With TDA1541 based CD players, the original system XTAL would have fed the filter chip (SAA7220) with an 11.2896Mhz clock. The clock would have been buffered and divided within the filter chip and redistributed around the player. The redistributed clock would be required at the decoder (SAA7210/SAA7350 etc) and DAC (TDA1541). Any noise on the filter chip would be injected into the clock as it passed through, degrading the quality of the redistributed clock and effecting potential performance.

Block diagram of basic clock distribution
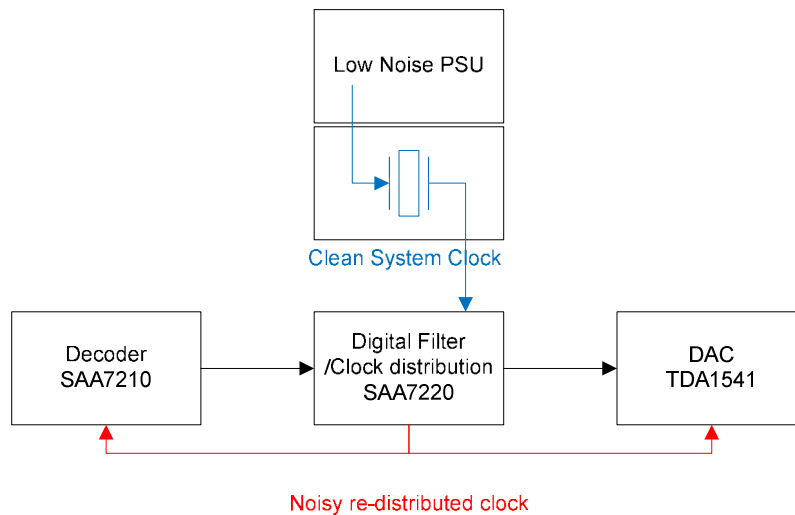
With the advanced clocking technique, we will look to provide multiple high quality clock signals to all the devices direct from the multiple C2 outputs.

Block diagram of advanced clock distribution
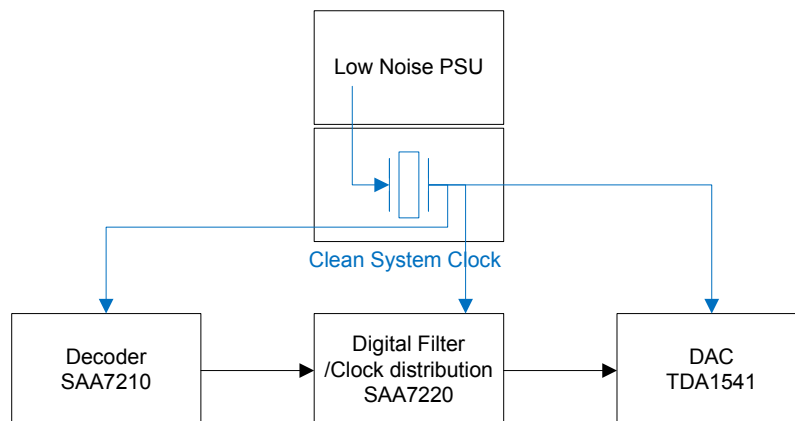
Performing the re-clock

For the purposes of complete re-clocking, we are concerned with the following clock frequencies:-

Master/System clock   11.2896Mhz

Bit Clock   5.6448Mhz (half the sys clock or /2)

Replacing std XTAL on SAA7220P/A or B digital filter

The standard crystal can be removed and replaced with the Master/System clock.

1. Carefully remove the clock related components (xtal, resistor & 2x ceramic caps)
2. Take a feed from the C2, X1 output and connect it to pin 11 (X-in). You take care to ensure that the connection is as close to the chip as possible. Usually you can connect where you have previously removed the resistor.
3. You should also disconnect the onwards supply (original clock distribution) by isolating pin 9 (Clock out pin).
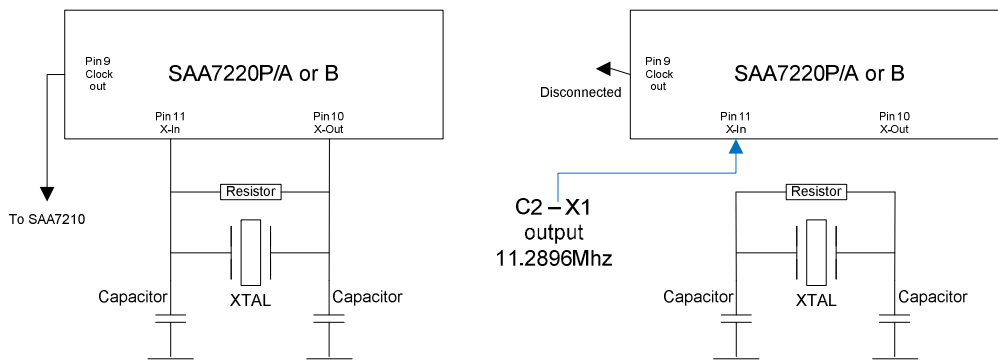
Replacing the clock feed on SAA7210 decoder

The decoder chip receives its system clock on pin 19. The clock is fed from pin 9 of the SAA7220P chip. The feed will have already been isolated in step 2 above. You should also isolate pin 19 locally.

1. Isolate pin 19 (clock in)
2. Take a feed from the C2, X1 output and connect it to pin 11 (X-in). You take care to ensure that the connection is as close to the chip as possible. As there are no components removed in this step, you will need to connect the feed directly to pin 19.
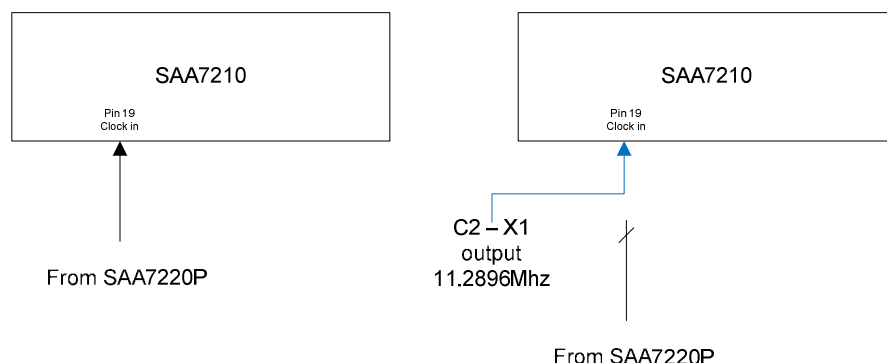
Replacing the bitclock feed on TDA1541

1. Cut the link between pin 2 & 4
2. Provide x1 clock to pin 4
     *this could also be tied to GND as an option
     *x1 clock may only work with nonA, S1 and S2 chips
3. Provide /2 to pin 2
     *May only work with nonA , S1 and S2

If you connect pin 4 to GND (Time multiplex mode), and you still have sound, it's obvious that this pin has no function in this mode (it's not used to clock the output latches).

However, it's possible that applying clock signals to pin4 (that is capacitively coupled to the TDA1541A internal circuits when not used), could affect on-chip interference levels, and I assume this would also be audible.

So the effect you are experiencing could be a change in interference levels at the DAC analogue outputs.

DEM reclock

It is not necessary to tie in to the voltage rail in order to perform the DEM reclock, but it will help with the overall stability of the circuit.

1. /2 clock to pin 17
2. Inverted/2 to pin 16

*if the DEM will not lock (distortion) reclock with /4 instead of /2 (due to chip tolerance).
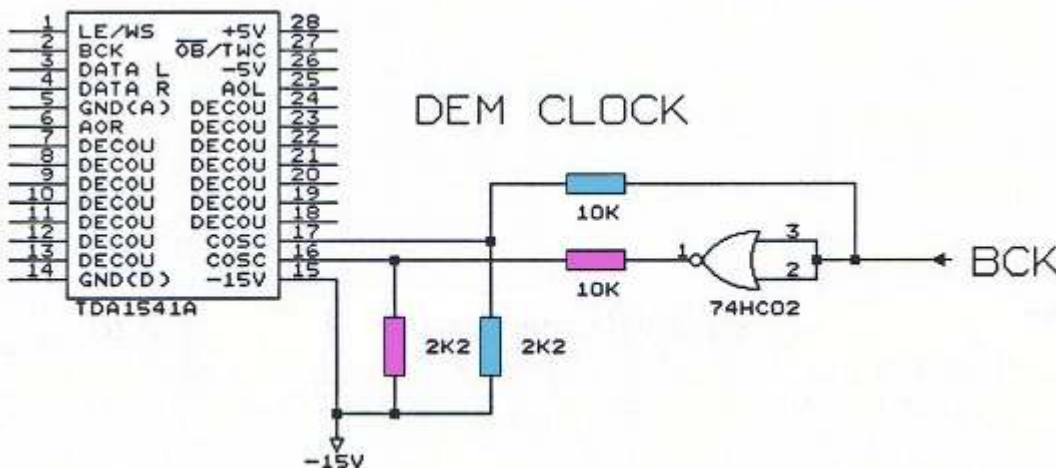
The DEM clock frequency has limits (max. frequency around 7 MHz), so 5.6448 MHz is close to the limit. It's better to decrease DEM clock to 2.8224 MHz. If the TDA1541A still doesn't sync (tolerances), the DEM clock frequency can be further reduced.

In order to make sure the DEM system works correctly, you have to test with low level recordings (Sheffield Lab / AT2B "My Disc"). When the DEM system syncs, sound should be crystal clear, when it doesn't, low level recordings sound highly distorted as bit errors increase significantly.

Reference ECDesigins http://www.diyaudio.com/forums/digital-line-level/79452-building-ultimate-nos-dac-using-tda1541a.html

Additional Bit Decoupling info

I attached part of the TDA1540 internal schematics (IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-14, NO. 3, JUNE 1979). TDA1541A schematics are similar, but this one has 10 passive current dividers and 6 active current dividers.

On the top right there is the current reference source, all binary weighted bit currents are derived (divided) from this reference current source. So if the output current of this current source changes (drift), all bit currents will change accordingly, preserving bit accuracy.

This constant current source also directly provides MSB current (2mA). It's mirrored against -15V, and then enters the first active divider (not shown).

There are 3 active dividers visible, they are driven through shift-register outputs A, B, C, and D. The speed the shift register is clocked, is determined by the DEM clock frequency.

Each active current divider consists of 4 transistors (passive divider) supplying 4 coarse (almost equal) currents to the switching matrix. The switching matrix connects each active divider output to each passive divider output alternatively, using a specific switching pattern. This way the active dividers perform time-averaging, meaning that the active divider outputs derive 4 closely matched output currents from 4 not so closely matched input currents. Two of these outputs are always tied together:

Example:

Input currents, 0.51mA, 0.48mA, 0.46mA, 0.49mA. After time averaging, 4 output currents are derived, each of these output currents equals (0.51 + 0.48 + 0.46 + 0.49) / 4 = 0.485mA. Since 2 outputs are connected, the output currents are 0.485mA, 0.485mA, and 0.97mA.

In other words, despite tolerances in the 4 passive divider input currents, the derived output currents will be closely matched due to time averaging. The currents are dynamically tuned to close tolerances.

There is a catch, if the time intervals between switching (DEM clock) vary, for example 5us, 0.49us, 5.1us, and 0.48uS, the passive divider tolerances aren't fully corrected, and bit errors occur. That's why it's important to keep the DEM clock jitter as low as possible as DEM clock jitter might result in higher bit errors.

Back to the TDA1541A-S2, running on the standard free running jittery DEM clock that prevents close matching of the 4 input currents. The only way to still get closely matched currents at the active divider output is to have equally close matched outputs on the passive dividers. Using above example:

Input currents, 0.485mA, 0.485mA, 0.485mA, 0.485mA. After time averaging (time intervals aren't equal), the output currents are still 0.485, 0.485, 0.485, 0.485.

The MSBs will have biggest impact on bit errors, the slightest errors here, and accuracy degrades quickly.

So the TDA1541A-S2 is only a plain TDA1541A that has slightly closer matching of the passive dividers that feed the switching matrix. So with the given jittery DEM clock, it still manages to provide slightly higher bit accuracy. But much more important, it will have lower ripple current on the active divider outputs too.

On the other hand, when we feed a plain TDA1541A chip with a highly accurate, low-jitter DEM clock that runs in sync with BCK, all DEM clock time intervals will be closely matched. This will result in similar performance as the S2 chip with closer passive divider current matching.

Passive divider tolerances also translate to increased ripple current on the active divider outputs. These outputs are filtered using an internal resistor, and an external decoupling capacitor (marked red).

The bigger the passive divider tolerances, the higher the ripple current amplitude. In order to prevent this, the DEM clock can be increased by approx. factor 10 (from approx. 200KHz to approx. 2.8224 MHz). Now it's easier to filter the active divider outputs and reduce ripple current (noise).
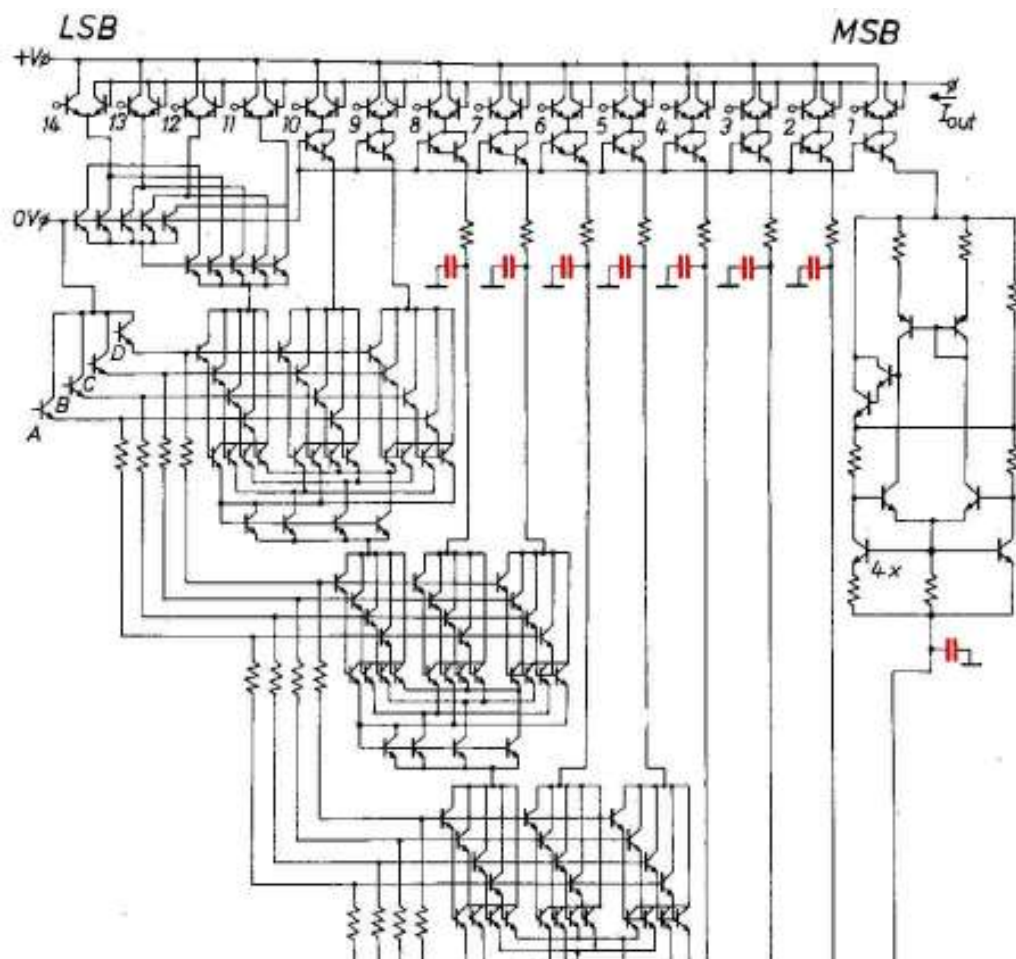
So TDA1541A performance can be significantly increased by ensuring DEM clock jitter is very low (equal time intervals), and DEM clock switching frequency is significantly increased (lower ripple current). Max. DEM clock frequency is limited to approx. 7 MHz,

Other factor that increases output current noise levels are the I2S signals. Even minute voltage fluctuations (ground-bounce) can affect the highly sensitive output signal. And since I/V conversion has to take place sooner or later, noise on the GND reference will degrade accuracy.

This is why it's very important to take whatever measures to minimize I2S induced ground-bounce. On chip, high-speed current steering logic is used (+/- 400mV levels), so here interference is already minimized.

In practice this means reducing I2S signal levels to approx. 400 ...600mVpp levels. The I2S inputs require a bias voltage of approx. 1 ... 1.4V, so this bias voltage has to be provided too. Using the SD-card player, it's possible to lower ground-bounce even further by using 32 bits / frame, resulting in 1.4112 MHz bit clock (ground-bounce decreases with decreased voltage and decreased frequency).

Recently I derived this bias voltage from the TTL level I2S signals, so bias voltage slightly varies with duty cycle (jitter). This affects the exact moment the TDA1541A will trigger, and it can be used to compensate for timing jitter, effectively reducing sample timing jitter. It's also important to interrupt the I2S TTL level signal current flow when it drops below approx. 1V, this is required to prevent full discharge of the I2S input stray capacitance, minimizing current surges. This new I2S jitter reduction circuit has resulted in most significant increase in TDA1543 / TDA1541A sound quality since I started this project.

Reference ECDesigns http://www.diyaudio.com/forums/digital-line-level/79452-building-ultimate-nos-dac-using-tda1541a.html

TDA1541A LSB current change equals 0.004 / 65536 = 61nA.

Active divider decoupling caps are directly connected between divider output and GND, so the slightest decoupling cap leakage current will change exact output current of 6 MSBs!

Typical tantalium cap leakage current (0.1uF ... 1uF) equals 500nA, so this will introduce up to 3-bit error on each of the MSBs. Leakage current also changes with other external factors like temperature and voltage. The tantalium caps should be ok for power supply decoupling.

Ceramic capacitors are microphonic (they will produce a small voltage when tapped, and will flex when a voltage is applied). High-K ceramic caps can produce audible sound when driven by a bias voltage with a super-imposed 1KHz sinewave for example. This makes them less suitable for audio applications.

Quote:

The active divider decoupling caps do have clearly audible effect on sound quality. The decoupling caps need to have low inductance, very low leakage current, and low microphonics. Some of the active divider outputs have only half the ripple frequency (check TDA1540 datasheet), and the ripple currents vary with the output current.

So capacitors filtering fDEM / 2 need to have twice the capacity of the capacitor filtering fDEM. fDEM is typically around 200 KHz. Capacitors filtering lower currents also have lower ripple current to filter, so capacitance can also be lower. When selecting capacitor values with respect to DEM clock ripple current frequency and active divider output current, and using 1uF as maximum value, following would apply:

pin 13,18, 2mA, fDEM /2, 1uF
pin 12,19, 1mA, fDEM, half current (13,18), twice the frequency of MSB, 250nF
pin 11,20, 0.5mA, fDEM / 2, half frequency, half current (12,19), 125nF
pin 10,21, 0.25mA, fDEM, half current double frequency (11,20), 31.25nF
pin 9,22, 0.125mA, fDEM / 2, half current, half frequency (10,21), 31.25nF
pin 8,23, 0.0625mA, fDEM, half current (9,22), 7,8nF
pin 7,24, 0.0625mA, fDEM, equal current (8,23), 7.8nF.

In practice, 1uF (MSB), 220nF, 120nF, 33nF, 33nF, 8.2nF, 8.2nF. This would give equal ripple currents on all MSBs.

Active divider decoupling also depends on DEM clock. Like mentioned before, DEM clock oscillator is able to "lock" on (on-chip) BCK crosstalk. By selecting DEM clock capacitor values that produce (almost) exact multiples of fs, the DEM clock will "lock" to BCK and jitter amplitude would drop significantly. The often used 470pF and 680pF won't result in a "lock" and produce maximum DEM clock jitter amplitude.

Here are some capacitor values that result in a "lock" condition, capacitance might vary slightly due to TDA1541A tolerances:

235.2 KHz, 350pF
256.58181 KHz, 318pF
282.24 KHz, 300pF
313.6 KHz, 260pF
352.8 KHz, 250pF
403.2 KHz, 203pF
470.4 KHz, 180pF
564.48 KHz, 145pF
705.6 KHz, 122pF

The capacitors need to have tight tolerance (1%).

Today I tested a new (more stable) external DEM clock circuit. It consists of a differential TTL-level clock source (352.8 or 705.6 KHz), and 4 resistors. each DEM clock pin (16 & 17) is connected to -15V through a 2K2 resistor. The TTL-level clock signals are connected to pin 16 & 17 using 10K Ohm series resistors. The resistors will provide bias voltage (prevents the internal DEM clock from oscillating), attenuation and level conversion. This is the best performing DEM clock circuit so far.

DEM clock operation must be tested with low level recordings (-40dB for example). Sheffield test CD "My Disc" contains such test tracks. When the DEM clock doesn't work, there is huge distortion, if it has spurious oscillations (usually around 7 MHz) sound quality will vary, but won't be optimal. Correct working DEM clock should produce a crystal clear sound. The fact that clock signals are measured on both pin 16 and 17 doesn't mean that the on-chip DEM clock oscillator actually functions. It can simply stop (no clock signal), or oscillate at different (higher) frequency.

Quote:

> and since only -15V is used in TDA as for this analog part

Unfortunately not, both +5V and -5V are also used for analogue circuits, in fact both +5V and -5V appear to be most critical. I had best results with approx. 3000uF (multiple caps in parallel) for power supply decoupling (TDA1541A).

Reference ECDesigns http://www.diyaudio.com/forums/digital-line-level/79452-building-ultimate-nos-dac-using-tda1541a.html

Additional CCS on output

Modified output stage with single Burson I/V stage